A MULTI-TERMINAL MODULAR MULTILEVEL CONVERTER-BASED HVDC SYSTEM WITH AN OFFSHORE WIND FARM

by

PUYU WANG

A thesis submitted to
The University of Birmingham
for the degree of
DOCTOR OF PHILOSOPHY

School of Electronic,
Electrical and Systems Engineering
The University of Birmingham
September 2015

UNIVERSITY OF
BIRMINGHAM

University of Birmingham Research Archive

e-theses repository

This unpublished thesis/dissertation is copyright of the author and/or third parties. The intellectual property rights of the author or third parties in respect of this work are as defined by The Copyright Designs and Patents Act 1988 or as modified by any successor legislation.

Any use made of information contained in this thesis/dissertation must be in accordance with that legislation and must be properly acknowledged. Further distribution or reproduction in any format is prohibited without the permission of the copyright holder.

To my wife and parents

ACKNOWLEDGEMENTS

First of all, I would like to express my deepest gratitude to my supervisor, Prof. Xiao-Ping Zhang. The guidance and support from him greatly helped me during my PhD study, particularly the kind encouragement and patient discussions when the research was not going well. Apart from the academic research, he also cared about my daily life. For me, it has been a true honour and privilege to be a student of Prof. Zhang. Without his guidance, the completion of the PhD study would have been impossible.

This PhD study was sponsored by UK EPSRC, UK National Grid and the School of EESE, University of Birmingham. I would like to greatly acknowledge and note my gratitude for the financial support.

I would like to thank my undergraduate supervisor, Prof. Mietek A. Brdys. Thanks to his professional and patient guidance, I was given the opportunity to carry on my PhD study. Also, I would like to thank for his academic advice for my research during my PhD study and suggestions for future work.

I would like to thank the English tutors and staff at the Birmingham International Academy, which was known as English for International Student Unit. The professional guidance and advice from them greatly improved my academic writing skill.

I would like to thank the staff at the Student Counselling Service, particularly Dr. David Mair, his professional guidance and kind advice during the counselling section greatly helped me during the hard time.

I would like to thank the technical support team of RTDS technologies. The professional

technical support from them helped improve my understanding and establish the simulation models.

I would like to thank Dr. Zhou Li and Dr. Dechao Kong, for their help at the initial stage of my PhD study. The collaboration with them placed a good basis for my further study. I would also like to thank Dr. Xuefeng Bai, Dr. Gan Li, Dr. Xuan Yang, Dr. Suyang Zhou, Dr. Jingchao Deng, Miss Rui Shi, Mr. Eduardo Pereira-Bonvallet, Mr. Jianing Li, Mr. Jing Li, Mr. Zhi Wu, Mr. Ying Xue, Ms. Can Li, Dr. Bo Yuan, Dr. Qiuyu Lu, Mr. Mao Li, Mr. Mingyu Xie, Mr. Hao Fu, Miss Conghuan Yang, Mr. Rui Guan, Miss Xianxian Zhao, and Mr. Jiajie Luo in the electrical power and control systems group. I greatly benefited from the discussions, their kind advices and assistance. It was very enjoyable working with them. I would also like to thank Mrs. Mary Winkles and Mrs. Samantha McCauley for their kind advice and support during my PhD study.

I must express my greatest appreciation for my wife, Ms. Na Deng. She always gives support, encouragement and understanding throughout my PhD study and gives me endless love. I must thank my parents, Prof. Jinquan Wang and Ms. Zhuanghua Bu, for their help and love in every way in my entire life.

ABSTRACT

The increased demand for electrical power and the concern of environmental pollution drive the development of bulk-power transmission over long distance and renewable energy. The use of multi-terminal (MT) modular multilevel converter (MMC) high-voltage direct current (HVDC) technology to integrate power from the offshore wind farm (OWF) is becoming increasingly popular. However, some technological barriers and potential risks may exist in the new technology, which requires comprehensive research and innovative developments.

This thesis investigates several important aspects of an offshore integrated MMC multi-terminal HVDC (MTDC) system, including start-up control, control and protection under AC and DC fault conditions. For the start-up control, a hierarchical start-up scheme is proposed for the terminals with active AC networks and a reduced DC voltage start-up scheme is proposed for the terminal with the OWF. Synthesising both schemes forms a comprehensive start-up control scheme for the start-up control of the MTDC system, which can effectively mitigate the voltage spikes and current surges during the start-up process. For control and protection against AC fault conditions, associated control and protection strategies and detailed control and protection sequences are proposed for the faults occurring at the converter AC-side. In addition, a special control and protection strategy is proposed when the faulted-side MMC experiences blocking failure following the fault. For the DC fault management, a fault isolation strategy is proposed and the system recovery scheme is comprehensively investigated after the fault isolation, with delayed-auto-re-configuration (DARC) schemes being proposed. Combining the DARC scheme and the fault isolation strategy, a complete control and protection sequence is proposed. Effectiveness of the proposed schemes is evaluated on the RTDS simulation platform.

TABLE OF CONTENTS

CHAPTER 1 INTRODUCTION 1

1.1 Research Background 1

1.1.1 HVDC Technologies 1

1.1.2 VSC HVDC Technology 3

1.1.3 Multi-terminal VSC HVDC 8

1.1.4 Offshore Wind Energy and its Integration 11

1.2 Literature Review 13

1.2.1 Simulation and Control of VSC HVDC Systems 13

1.2.2 Start-Up Control of VSC HVDC Systems 19

1.2.3 Control and Protection of VSC HVDC under AC Fault Conditions 22

1.2.4 Control and Protection of VSC HVDC under DC Fault Conditions 26

1.3 Research Objectives and Contributions 32

1.3.1 Start-Up Control 32

1.3.2 Control and Protection against AC Faults 33

1.3.3 Control and Protection against DC Faults 33

1.4 Thesis Outline 34

CHAPTER 2 CONFIGURATION, STRUCTURE AND CONTROL OF THE MMC MTDC SYSTEM WITH AN OWF 37

2.1 Introduction 37

2.2 System Configuration 37

2.3 MMCs 38

2.3.1 Structure 39

2.3.2 Operating Mode at Valve Level 41

2.3.3 Control Mode at Converter Level 48

2.3.4 Reference Settings at System Level 52

2.4 Offshore Wind Farm 52

2.4.1 DFIG Structure 53

2.4.2 Basic Control Strategy of a DFIG 54

2.5 Summary 56

CHAPTER 3 STEADY-STATE, POWER BALANCING AND POWER FLOW REVERSAL OF THE MMC MTDC SYSTEM WITH AN OWF 57

3.1 Introduction 57

3.2 Steady-State Condition 57

3.2.1 Nominal Steady-State Calculation 57

3.2.2 Transient Assumption 58

3.3 Transient Conditions between Two Steady-States 59

3.3.1 Change of Wind Speed 59

3.3.2 Wind Intermittency 63

3.3.3 Power Ramping 65

3.3.4 Power Flow Reversal 68

3.4 Summary 71

CHAPTER 4 START-UP CONTROL OF THE MMC MTDC SYSTEM WITH AN OWF 72

4.1 Introduction 72

4.2 Start-Up Process and Control of the Onshore Terminals with Active AC Networks 73

4.2.1 Before the Deblocking of the MMCs 73

4.2.2 After the Deblocking of the MMCs 77

4.2.3 Hierarchical Start-Up Control Scheme 79

4.3 Start-Up Process and Control of the Offshore MMC with Passive AC Network 81

4.3.1 Before the Deblocking of MMC-1 82

4.3.2 After the Deblocking of MMC-1 85

4.3.3 Comprehensive Start-Up Control Sequence 86

4.4 Simulation Case Studies 88

4.4.1 Case A 89

4.4.2 Case B 94

4.4.3 Case C 99

4.4.4 Discussion and Comparison of the 3 Cases 103

4.5 Summary 105

CHAPTER 5 CONTROL AND PROTECTION OF THE MMC MTDC SYSTEM WITH AN OWF AGAINST AC FAULTS 107

5.1 Introduction 107

5.1.1 General Control and Protection and Some Definitions 107

5.1.2 Control and Protection against AC Faults 108

5.2 Control and Protection Against the Converter-Side AC Fault at the Power Regulated Terminal 110

5.2.1 Fault Characteristics and Fault Isolation 111

5.2.2 Faulted Section Isolation 112

5.2.3 Control and Protection Sequence 113

5.2.4 Simulation Case Study 114

5.3 Control and Protection against the Converter-Side AC Fault at the Master Terminal 117

5.3.1 Fault Characteristics and Fault Isolation 117

5.3.2 Faulted Section Isolation 119

5.3.3 Control and Protection Sequence 120

5.3.4 Simulation Case Study 122

5.4 Control and Protection Against Converter-Side AC Fault with the Faulted-Side MMC Blocking Failure 126

5.4.1 Whole MMC Blocking Failure 127

5.4.2 One Converter Arm Complete Blocking Failure 135

5.4.3 One Converter Arm Partly Blocking Failure 137

5.4.4 Discussion 148

5.5 Summary 148

CHAPTER 6 CONTROL AND PROTECTION OF THE MMC MTDC SYSTEM WITH AN OWF AGAINST DC FAULTS 151

6.1 Introduction 151

6.1.1 Comparison between DC Fault Isolation and AC Fault Isolation 152

6.1.2 DC Fault Isolation Schemes 153

6.1.3 System Recovery after Faulted Section Isolation 155

6.1.4 DC Fault at Different Locations 155

6.2 Control and Protection Against the DC Fault at the Power Regulated Terminal 156

6.2.1 Fault Characteristics and Fault Isolation 156

6.2.2 Faulted Section Isolation 159

6.2.3 System Recovery 160

6.2.4 Control and Protection Sequence 165

6.2.5 Simulation Case Study 167

6.3 Control and Protection Against the DC Fault at the Master Terminal 175

6.3.1 Fault Characteristics and Fault Isolation 175

6.3.2 Faulted Section Isolation 177

6.3.3 System Recovery 177

6.3.4 Control and Protection Sequence 181

6.3.5 Simulation Case Study 183

6.4 Summary 191

CHAPTER 7 CONCLUSIONS AND FUTURE WORK 194

7.1 Conclusions 194

7.2 Future Work 199

APPENDIX A 203

A.1 Configuration of the MTDC Test System 203

A.2 Measuring Points of the System in the Simulations 204

A.3 Parameters of the MTDC Test System 205

APPENDIX B 206

B.1 MMC Models in the RTDS 206

B.1.1 Average Model of MMC 206

B.1.2 Detailed Switching Model of MMC 207

B.2 Mathematical Representation of MMC 208

APPENDIX C 214

C. Mechanical Model for Wind Turbine 214

APPENDIX D **216**

D. Calculation of Fault Current **216**

PUBLICATIONS AND OUTCOMES **219**

LIST OF REFERENCES **221**

LIST OF FIGURES

Figure 1-1 Typical topologies of VSCs: (a) 2-level VSC; (b) 3-level VSC [16]-[18] 4

Figure 1-2 Topology of the half-bridge MMC [17], [19]-[20] 5

Figure 1-3 Maximum power by the year of commissioning of VSC HVDC projects [24] 7

Figure 1-4 Topology of FBSM and CDSM: (a) FBSM; (b) CDSM [27]-[29] 8

Figure 1-5 Radial and meshed topologies of a 3-terminal HVDC grid: (a) Radial topology; (b) Meshed topology 10

Figure 1-6 Comparison of the energy generation sources in 2009 and the target in 2020 [43] 12

Figure 1-7 *dq* decoupled control 17

Figure 1-8 V_{ac}-*f* control 17

Figure 2-1 Configuration of the OWF integrated 4-terminal MMC HVDC system 37

Figure 2-2 System level, converter level and valve level control of an MMC 39

Figure 2-3 Structure of an MMC 40

Figure 2-4 Structure of a 2-level VSC 41

Figure 2-5 Equivalent circuit diagram of an MMC 43

Figure 2-6 (a) Modulation of a 2-level square wave; (b) Modulation of a staircase wave 43

Figure 2-7 Control diagram of NLM in the RTDS 44

Figure 2-8 Capacitor balancing control in the RTDS 46

Figure 2-9 Inner current controller of the *dq* decoupled control 48

Figure 2-10 Outer controller of the *dq* decoupled control 49

Figure 2-11 V_{ac}-f control 51

Figure 2-12 Structure of one DFIG [125]-[126] 54

Figure 2-13 LVRT requirement [130] 55

Figure 3-1 Measuring points of the MTDC 60

Figure 3-2 System performance under changes of wind speed 62

Figure 3-3 System performance under intermittent wind condition 65

Figure 3-4 System performance under power ramping 68

Figure 3-5 System performance under power flow reversal 70

Figure 4-1 System state before start-up 72

Figure 4-2 System state after closing the AC circuit breaker 74

Figure 4-3 MMC with blocked state [86], [133] 74

Figure 4-4 Equivalent RLC circuit before deblocking of the MMC: (a) equivalent circuit, (b) simplified circuit 75

Figure 4-5 Equivalent representation of the SMs in an MMC after deblocking [133] 77

Figure 4-6 Voltage change of a SM from the initial state to the steady-state [133] 78

Figure 4-7 Hierarchical start-up control of the terminals with active AC networks 80

Figure 4-8 State of T1 before the deblocking of MMC-1 82

Figure 4-9 Initial charging loop of MMC-1 before deblocking [86], [133] 83

Figure 4-10 Equivalent circuit before deblocking MMC-1: (a) equivalent circuit, (b)

simplified circuit 84

Figure 4-11 Capacitor voltage change of a SM 85

Figure 4-12 System start-up performance using the proposed start-up control sequence 93

Figure 4-13 System start-up performance using the start-up control sequence without reduced DC voltage control 97

Figure 4-14 Comparison of the system start-up performance of Case A and Case B: (a) Capacitor voltage of MMC-1; (b) DC current at T1 99

Figure 4-15 System start-up performance using the start-up control sequence without any changes on the voltage and power settings 102

Figure 5-1 Comprehensive process of control and protection against a fault 107

Figure 5-2 Three-phase to ground fault at the AC-side of MMC-1 111

Figure 5-3 Fault isolation by blocking of MMC and tripping of AC circuit breaker 112

Figure 5-4 Faulted section isolation 112

Figure 5-5 Control and protection sequence against AC fault at the AC-side of MMC-1 113

Figure 5-6 System performance under an AC fault at the AC-side of MMC-1 using the proposed control and protection sequence 116

Figure 5-7 AC fault occurs at the AC-side of MMC-2 118

Figure 5-8 Control and protection strategy for the fault isolation 118

Figure 5-9 System status after the fault isolation at the master terminal 119

Figure 5-10 System status after the faulted section isolation at the master terminal 119

Figure 5-11 Comprehensive control and protection sequence under AC fault at MMC-2 AC-

side 120

Figure 5-12 System state after the recovery of the unfaulted terminals 122

Figure 5-13 System performance under an AC fault at the AC-side of MMC-2 using the proposed control and protection sequence 124

Figure 5-14 System state at T1 after the fault under MMC-1 completely blocking failure 127

Figure 5-15 Performance of the AC-side RMS current of MMC-1 under MMC-1 AC-side fault with MMC-1 complete blocking failure using the basic control and protection sequence 128

Figure 5-16 System status with special control and protection to achieve the fault isolation 130

Figure 5-17 System state with special control and protection to achieve the faulted section isolation 130

Figure 5-18 Special control and protection sequence for the fault isolation and faulted section isolation under AC fault at MMC-1 AC-side with complete blocking failure of MMC-1 131

Figure 5-19 System performance under an MMC-1 AC-side fault with complete blocking failure of MMC-1 using the proposed special control and protection 133

Figure 5-20 System status at T1 with one arm complete blocking failure of MMC-1 135

Figure 5-21 Performance of the AC-side RMS current of MMC-1 under the fault with MMC-1 one arm complete blocking failure using the basic control and protection sequence 136

Figure 5-22 System status at T1 with one arm partly blocking failure of MMC-1 in which only 1 SM is blocked successfully 137

Figure 5-23 System performance under an MMC-1 AC-side fault with one arm of MMC-1

partly blocking failure (1 SM blocked successfully) using the basic control and protection 139

Figure 5-24 System status at T1 with one arm partly blocking failure of MMC-1 in which half of the SMs are blocked successfully 142

Figure 5-25 System performance under an MMC-1 AC-side fault with one arm of MMC-1 partly blocking failure (half SMs blocked successfully) using the basic control and protection 144

Figure 5-26 System status at T1 with one arm partly blocking failure of MMC-1 in which only 1 SM has blocking failure 145

Figure 5-27 System performance under an MMC-1 AC-side fault with one arm of MMC-1 partly blocking failure (1 SM blocked unsuccessfully) using the basic control and protection 147

Figure 6-1 DC pole-to-pole fault on DC Cable 1 157

Figure 6-2 System state with blocking all MMCs 157

Figure 6-3 Current flow in a blocked MMC under the DC fault 158

Figure 6-4 System status with fault isolation strategy 159

Figure 6-5 System status after faulted section isolation 159

Figure 6-6 Process of DARC scheme 165

Figure 6-7 Comprehensive control and protection sequence under DC fault on DC Cable 1 165

Figure 6-8 System state after the recovery of the unfaulted terminals 167

Figure 6-9 System performance under an DC fault on DC Cable 1 using proposed control and

protection sequence 169

Figure 6-10 Different control and protection sequence under DC fault on DC Cable 1 171

Figure 6-11 System performance under an DC fault on DC Cable 1 using a different control and protection sequence at the system recovery phase 173

Figure 6-12 DC pole-to-pole fault on DC Cable 2 176

Figure 6-13 System state with fault isolation strategy 176

Figure 6-14 System state after the faulted section isolation 177

Figure 6-15 Process of modified DARC scheme 180

Figure 6-16 Comprehensive control and protection sequence under DC fault on DC Cable 2 181

Figure 6-17 System state after the recovery of the unfaulted terminals 182

Figure 6-18 System performance under an DC fault on DC Cable 2 using proposed control and protection sequence 185

Figure 6-19 Control and protection sequence under DC fault on DC Cable 2 with the MTDC using voltage droop control 187

Figure 6-20 System performance with droop control mode under an DC fault on DC Cable 2 using proposed control and protection sequence 190

Figure A-1 Configuration of the OWF integrated 4-terminal MMC HVDC system 203

Figure A-2 Measuring points of the MTDC 204

Figure B-1 Average model of the MMC in the RTDS library – MMC4 206

Figure B-2 Detailed switching model of the MMC in the RTDS library – MMC ChainV3

207

Figure B-3 Modelling of one phase of MMC [131], [151] 209

Figure D-1 System Performance under MMC-1 AC-side fault with MMC-1 complete blocking failure using the basic control and protection sequence 217

LIST OF TABLES

Table 1-1 Typical VSC HVDC applications [24] 6

Table 1-2 Current Commissioned MTDC Projects 9

Table 2-1 Operating Modes of a SM 47

Table 2-2 Control Modes of the MMCs 51

Table 2-3 Control Reference Settings of the MMCs 52

Table 2-4 Control Strategy of the DFIG 54

Table 3-1 System Status under the Nominal Steady-State Condition 58

Table 4-1 Hierarchical Start-Up Control Scheme for the Master Terminal T2 [133] 80

Table 4-2 Hierarchical Start-Up Control Scheme for the Terminals with Active AC Networks 81

Table 4-3 Start-Up Control Scheme for the Terminal with OWF 85

Table 4-4 Comprehensive Start-Up Control Scheme for the Offshore Integrated MMC MTDC 86

Table 4-5 Comparison of the Start-Up Control of 3 Cases 89

Table 4-6 Description of the Operational Time of the Proposed Control Sequence 89

Table 4-7 Comparison of the Start-Up Control Performance of 3 Cases 104

Table 5-1 Description of the Operation and Timing of the Control and Protection Sequence in Figure 5-5 114

Table 5-2 Description of the Control and Protection Sequence in Figure 5-11 121

Table 5-3 Description of the Control and Protection Sequence in Figure 5-18 131

Table 6-1 Comparison of the Number of Electric Components between Half-bridge MMC, Full-bridge MMC and C-MMC [30] 154

Table 6-2 Description of the Control and Protection Sequence in Figure 6-7 166

Table 6-3 Description of the Control and Protection Sequence in Figure 6-10 171

Table 6-4 Description of the Control and Protection Sequence in Figure 6-16 181

Table 6-5 Description of the Control and Protection Sequence in Figure 6-19 187

Table A-1 Parameters of the MTDC Test System 205

LIST OF ABBREVIATIONS

AAC	Alternate Arm Converter
AVM	Average Value Model
DARC	Delayed-Auto-Re-Configuration
DFIG	Doubly-Fed Induction Generator
DS	Director Switches
ESS	Energy Storage Systems
FACTS	Flexible AC Transmission System
FBSM	Full-Bridge Sub-Module
FRT	Fault Ride-Through
HBSM	Half-Bridge Sub-Module
HCMC	Hybrid Cascaded Multilevel Converter
HVAC	High Voltage Alternating Current
HVDC	High Voltage Direct Current
IG	Induction Generator
IGBT	Insulated-Gate Bipolar Transistor
KVL	Kirchhoff's Voltage Law
LCC	Line Commutated Converter
LVRT	Low Voltage Ride-Through
MMC	Modular Multilevel Converter
MTDC	Multi-Terminal HVDC
OWF	Offshore Wind Farm
PCC	Point of Common Coupling
RTDS	Real-Time Digital Simulator

SM	Sub-Module
VSC	Voltage Source Converter

CHAPTER 1 INTRODUCTION

As the 1st chapter of the thesis, the objectives are: 1) to introduce the research background and the current development of HVDC technologies, so as to reveal the importance and necessity of the research project; 2) to conduct an in-depth literature review of the related research publications to present the current state-of-the-art technologies and to identify potential innovations; 3) to describe the research objectives of the thesis and to present the original contributions; 4) to outline the chapters of the thesis.

1.1 Research Background

1.1.1 HVDC Technologies

The debates on the best technology for electrical power transmission, AC or DC, have been on-going since the "War of Currents" in the late 1880s. Although the technology of AC power grids nowadays is relatively mature and has been widely applied and accepted, it cannot prevent the pace of progress of the development of the high-voltage direct current (HVDC) technologies. Since the commissioning of the world first commercial HVDC link between mainland Sweden and the island of Gotland in 1954 [1], there have been over 200 HVDC projects that have been projected and commissioned worldwide [2].

The development of HVDC technologies is fundamentally driven by the rapidly increasing demand for electrical energy and thanks to the innovations and breakthrough of power electronic devices with reduced losses and costs. Technologically, the rapid development of HVDC technologies is mainly because of its advantages in comparison with using high-voltage alternating current (HVAC) [3]–[4], such as suitability for long-distance bulk-power

transmission and interconnection of asynchronous AC systems, having no distance effect on stability, suitability for remote and offshore integration, low transmission line losses and the low line footprint.

The key component in an HVDC is the converter stations in which the core devices are the power electronic switching valves. Mercury arc valves were the first generation to be used in HVDC applications, such as in the world first commercial HVDC link project [1]. With the development of power electronic devices, the emergence of thyristor valves in 1957, which overcame the drawbacks of mercury valves [5] of arc backs, high maintenance and long start-up time, gradually replaced the use of mercury valves and have become the core components in HVDC applications since then. After several decades, the emergence of the fully-controlled power electronic devices and the proposal of introducing them, such as insulated-gate bipolar transistor (IGBTs), into HVDC technologies have promoted the applications of HVDC into a new era [6]–[7].

The current HVDC technologies can be generally divided into 2 types [4]: one is the conventional thyristor-based line commutated converter (LCC) HVDC, while the other is the IGBT-based voltage source converter (VSC) HVDC. Due to the fact that the development and maturity of thyristor technology preceded IGBT technology, the current operational HVDC applications mostly use LCC HVDC technology. However, the performance of VSC HVDC is much more flexible than that of LCC HVDC due to its intrinsic control characteristics [7] and not having the problem of commutation failure, which is a significant problem with LCC HVDC. There have been some LCC HVDC projects in which the inverter-side is replaced by VSC to avoid the commutation failure and a number of HVDC projects nowadays apply VSC HVDC technology [8]–[10]. It can be anticipated that VSC HVDC technology will gradually

replace the conventional HVDC with the technical development.

1.1.2 VSC HVDC Technology

In comparison with the thyristor valve used in LCC HVDC, the IGBTs used in VSC HVDC can both be turned on and turned off and its commutation does not rely on the line voltage. Hence, VSC is also named as a self-commutated converter. Due to its flexible characteristics in HVDC transmission, it is anticipated that this technology will have wide and promising applications in the future and 4 main world leading manufacturers of electrical equipment have registered names for their VSC HVDC techniques, namely, HVDC Light by ABB [11], HVDC PLUS by Siemens [12], HVDC MaxSine by Alstom [13], and HVDC Flexible by State Grid Corporation of China [14]. VSC HVDC has independent control of active and reactive power, having no requirement of reactive power compensation and hence fewer AC filters are needed, easy implementation of power flow reversal by reversing the direction of DC current, facilitation of multi-terminal HVDC (MTDC) grid establishment, capability of connecting/supplying weak or passive AC network and black start capability [7].

For VSC HVDC technology, it can have different variants according to its topology [15]. The traditional and commonly known topologies are the 2-level VSC as shown in Figure 1-1(a) and multilevel VSCs as shown in Figure 1-1(b) which depicts the topology of a 3-level VSC. [16]–[18]

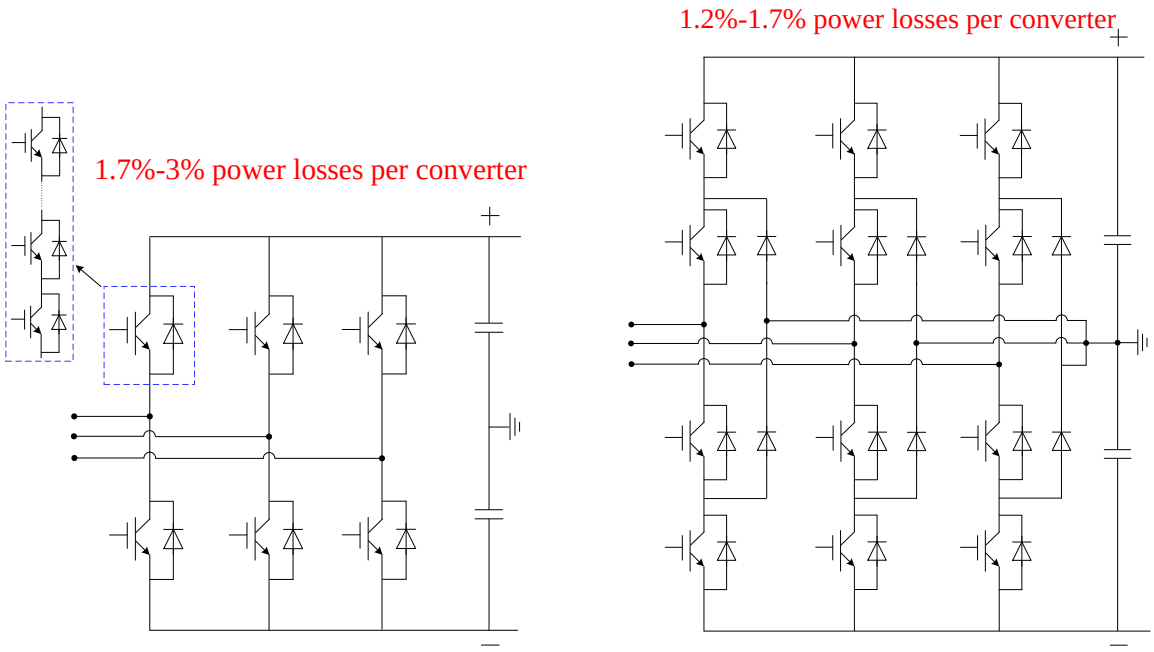


Figure 1-1 Typical topologies of VSCs: (a) 2-level VSC; (b) 3-level VSC [16]-[18]

In comparison with the traditional 2-level and 3-level VSCs, the current state-of-the-art technology modular multilevel converter (MMC) VSC, whose topology was proposed in 2001 [12], is considered to be the most promising topology and its advantages have now been widely recognised. Figure 1-2 depicts the topology of the MMC.

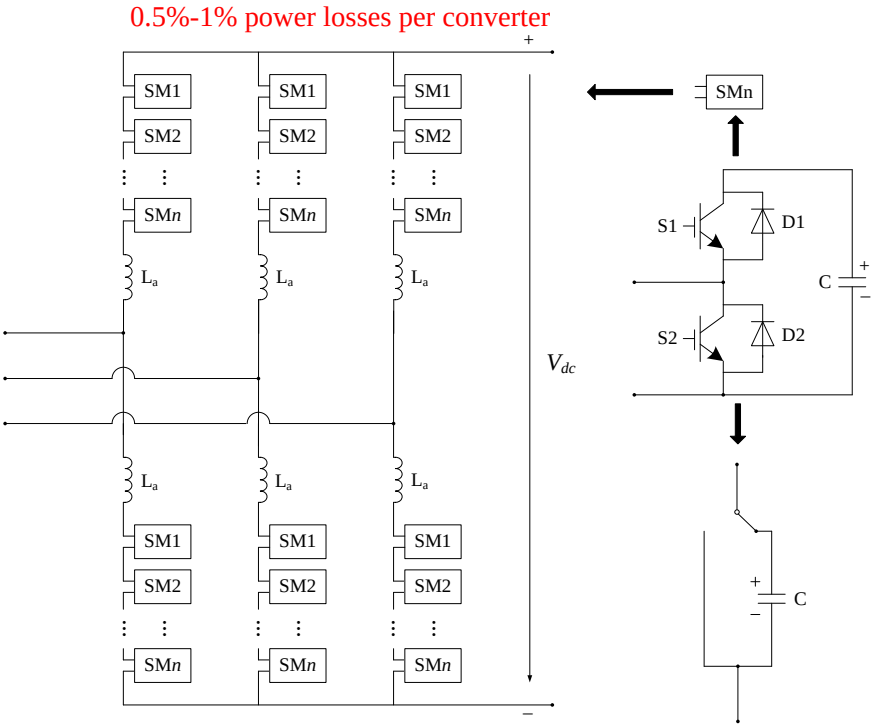


Figure 1-2 Topology of the half-bridge MMC [17], [19]-[20]

Figure 1-2 shows the standard topology of the MMC, also known as the half-bridge MMC. In comparison with the previous 2&3–level VSC, each valve of the MMC, also known as sub-modules (SMs), becomes an actual controllable voltage source in its own right [21] rather than a simple switch. Hence, it does not require synchronous switching operations of the cascaded valves [22] and the switching frequency can be much lower while maintaining the performance of the modulated wave at the converter AC-side [18]. The switching frequency of an MMC can be as low as 150 Hz which is three times of the fundamental frequency [23], while for the traditional 2&3–level VSC, the switching frequency is generally as high as 1-2 kHz [18]. The switching losses of MMC are significantly reduced with the reduction of the switching frequency. Since the switching losses occupy a large proportion of the converter power losses, which mainly consist of conduction losses and switching losses [16]–[18], the total power losses of MMC are significantly reduced. However, for the traditional VSC,

power losses are considered to be a marked drawback compared with those of LCC [17]. Figure 1-1 and Figure 1-2 also show the average power losses of the VSCs [16]–[20]. In addition, another drawback of the traditional VSC is the lower converter rating compared with that of LCC, since the rating of IGBTs is generally lower than that of thyristors. Thanks to high modularity of the MMC, the rating of the converter can be extended by simply increasing the number of SMs [22]. Moreover, owing to the development of IGBTs, the ratings of IGBTs have been greatly enhanced. Table 1-1 lists some typical VSC HVDC applications [24].

Table 1-1 Typical VSC HVDC applications [24]

Project	**Country**	**Year**	**Topology**	**Power**	**Voltage**	**Supplier**
Hallsjon	Sweden	1997	2-level	3 MW	± 10 kV	ABB
Gotland	Sweden	1999	2-level	50 MW	± 80 kV	ABB
Terranora	Australia	2000	2-level	180 MW	± 80 kV	ABB
Cross Sound	US	2002	3-level	330 MW	± 150 kV	ABB
Estlink	Finland	2006	2-level	350 MW	± 150 kV	ABB
Trans Bay Cable	US	2010	MMC	400 MW	± 200 kV	Siemens
East West Link	Australia	2012	MMC	500 MW	± 200 kV	ABB
Tres Amigas	US	2014	MMC	750 MW	± 345 kV	Alstom
DolWin2	Germany	2015	MMC	900 MW	± 320 kV	ABB

A clear increasing trend of the ratings of VSC HVDC can be observed in Table 1-1 and can be visibly observed in the maximum power by the year of commissioning drawn in Figure 1-3. [24]

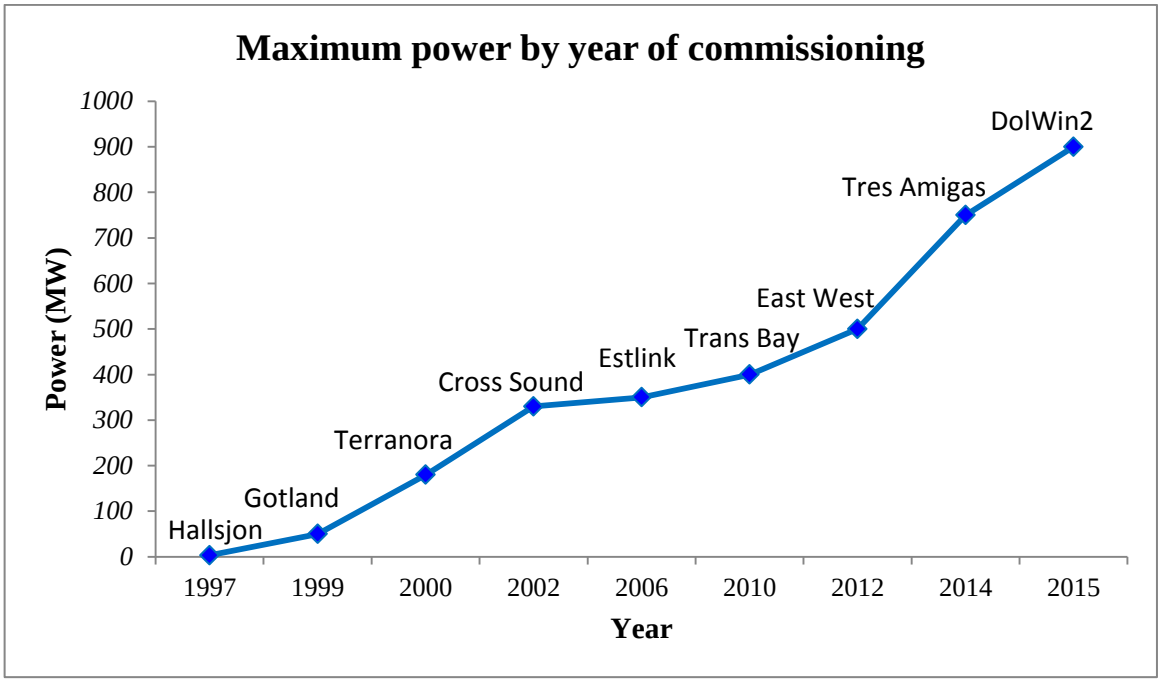


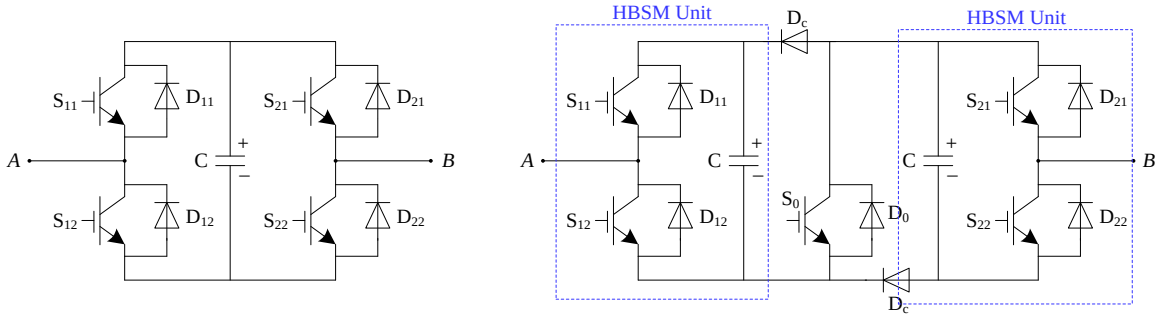
Figure 1-3 Maximum power by the year of commissioning of VSC HVDC projects [24]

Apart from low switching frequency, low power losses and high modularity, MMC has other salient features [22] such as high availability, high reliability, having no requirement on filters, small footprint, easy replacement of the existing components.

With these features, MMC is one of the ideal candidates for HVDC, including MTDC applications [8], [25]. Its first application was on the "Trans Bay Cable" project [10] in the US between the East Bay and San Francisco with a rating of ±200 kV, 400 MVA as shown in Table 1-1 with 200 SMs per converter arm. The project was commissioned in 2010. Table 1-1 also lists other 3 projects using MMC HVDC technology.

The standard topology of MMC is the half-bridge MMC as shown in Figure 1-2. However, similar to most traditional VSC topology, the half-bridge MMC cannot effectively isolate DC fault currents and necessitates tripping of the AC circuit breakers at the adjacent terminals [26]. In order to achieve DC fault isolation by the control of the converter itself, different

MMC topologies have been developed using the standard 1st type half-bridge MMC topology, with the emergence of the 2nd type MMC topology [27]–[29], which applies full-bridge SMs (FBSMs) or clamp double SMs (CDSMs) as shown in Figure 1-4.



(a) (b)

Figure 1-4 Topology of FBSM and CDSM: (a) FBSM; (b) CDSM [27]-[29]

The DC fault current can be blocked through effective control of the SMs. However, compared with the half-bridge SMs (HBSMs), the 2nd type of the MMC topology requires more power electronic devices, which increases the operational losses and costs [30]. In order to achieve both objectives of isolating the DC fault current and increasing relative fewer number of power electronic devices, a 3rd type of MMC topologies has emerged [31]–[32] and is a combination of series 2-level IGBTs namely the director switches (DS), and the FBSMs, such as the alternate arm converter (AAC) [31] and hybrid cascaded multilevel converter (HCMC) [32]. The 3rd MMC generation has DC fault blocking capability while the number of semiconductor switches required is lower than that of the 2nd generation.

1.1.3 Multi-terminal VSC HVDC

The term multi-terminal HVDC [33] mainly refers to an HVDC topology in which the DC buses of three or more HVDC converters are connected to a common DC grid regardless of whether the associated AC grids are synchronous or not. Similar to AC power grids, the

intention of establishing HVDC grids, which is multi-terminal DC grids, will naturally emerge when the technology of HVDC grows to a high maturity. This is because in comparison with the traditional 2-terminal HVDC link, MTDC has higher utilisation of DC lines, higher reliability of power supply and the DC network becomes more flexible [33]–[34]. For example, when a permanent fault occurs in an MTDC grid, with effective control and protection actions, the unfaulted terminals may keep operation without interruption [35]. However, for the same fault occurring in a 2-terminal HVDC grid, it may cause the interruption of the whole HVDC network.

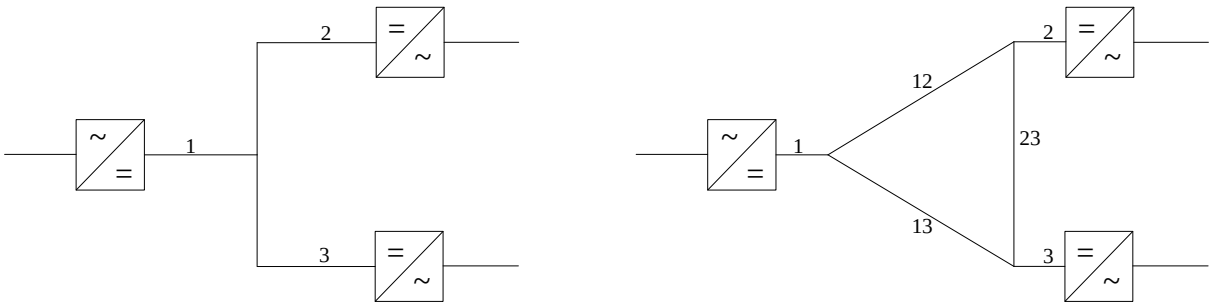
In comparison with the LCC technology, the VSC technology is more appropriate for the applications of MTDC. This is due to its flexible control characteristics and the fact that the power flow reversal can be easily achieved by reversing the direction of DC currents without the need to change the polarity of the DC voltage [7]. Compared with the traditional VSC, the use of MMC is considered to be more attractive for MTDC applications, due to its inherent characteristics and low failure rates [22]. Three MTDC projects have been commissioned recently and they all utilise the state-of-the-art technology, MMC, as shown in Table 1-2.

Table 1-2 Current Commissioned MTDC Projects

Project	**Country**	**Year**	**Topology**	**Power**	**Voltage**	**Terminals**
Nan'ao	China	2014	MMC	200 MW	±160 kV	3
Zhoushan	China	2014	MMC	400 MW	±200 kV	5
Tres Amigas	US	2014	MMC	750 MW	±345 kV	3

Topologies of MTDC generally consist of radial topology and meshed topology [8], [36]. In the radial topology there is only 1 path between any two electrical nodes, while in the meshed

topology there are two or more paths between two electrical nodes [36]. The simplest MTDC configuration is a 3-terminal HVDC. Figure 1-5 presents a simple representation of the radial topology and meshed topology of a 3-terminal HVDC grid.



(a) (b)

Figure 1-5 Radial and meshed topologies of a 3-terminal HVDC grid: (a) Radial topology; (b) Meshed topology

Both topologies have their merits and drawbacks. For the radial topology, since there is only 1 branch between 2 converter stations, the DC power can be fully controlled by the converters. However, when a permanent DC fault occurs at a terminal, the converter station at the faulted terminal cannot continue operation. For the meshed topology, when the same fault occurs at a terminal, the converters can resume operation via an alternative path after the fault isolation. However, the drawback of this topology is that since there are 2 or more branches between 2 converter stations, the complete control of the DC power cannot be achieved by controlling the converter itself and necessitates the installation and control of additional components such as DC-DC converters [36]. However, since the cost of DC-DC converters is considerable [37], the radial topology is applied by most MTDC applications.

In comparison with the traditional 2-terminal HVDC, the configuration and control of MTDC becomes more complex. The coordination control of each terminal becomes important to ensure the system operation in a stable manner, which includes both the steady-state and

dynamic conditions [38]–[40]. For the control strategies of MTDC systems, 2 main control paradigms [33], [38]–[41] are generally utilised, i.e. master-slave control [33] and voltage droop control [38]–[41]. Under steady-state condition, the balance of the power transfer in the MTDC should be maintained. Under dynamic conditions, stable start-up of the MTDC should be achieved by appropriate start-up control; effective control and protection of the system after AC and DC fault conditions, including system recovery after the fault isolation, should be achieved by appropriate control and protection sequences.

1.1.4 Offshore Wind Energy and its Integration

Due to the overutilization of conventional energy in the last several decades, environmental problems, particularly the over emission of carbon dioxide and the potential risk of shortage of conventional energy, have become prominently apparent, which drives more attention on effective exploitation and deployment of renewable energy. Regarding the electrical power generation, many countries have put forward strategic targets on the energy consumption from renewable energy sources [42]–[44] such as wind energy, solar energy and marine energy. Taking the UK as an example, a target was set in 2009 to achieve the generation of 15% of its energy demand from renewable sources by 2020 [43]. If the target is achieved by 2020, a scope of generating 30%-45% of all energy consumed from renewables may be reached by 2030 and the final target is to reduce CO_2 emissions by 80% by 2050 with regards to 1990 levels [43]–[45]. The reduction of CO_2 emissions brings benefits for the environment by replacing traditional energy to renewable energy. However, renewable generation sources that cannot provide sufficient inertia to support the power grid still remain a challenge and need solutions, e.g. installation and control of more energy storage systems (ESS) and more interconnections by using HVDC, to be put forward. Figure 1-6 illustrates the comparison of

electricity generation sources in 2009 and the target of those in 2020 [43]. In [43], "other sources" are not specifically defined and they may include HVDC interconnections and ESS.

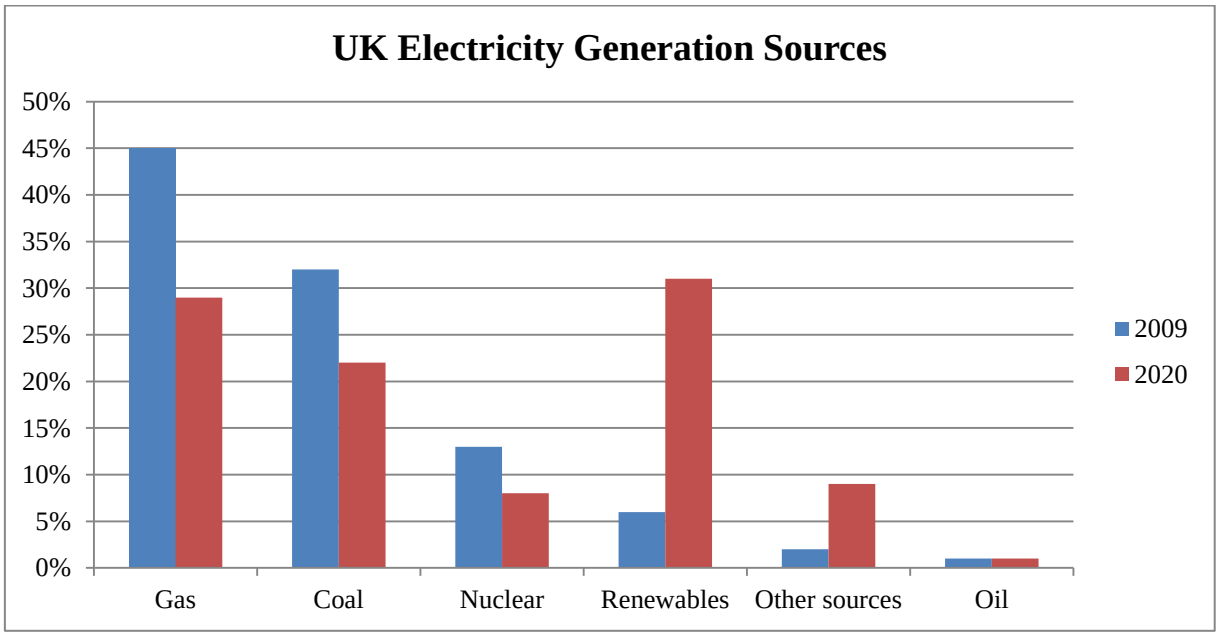


Figure 1-6 Comparison of the energy generation sources in 2009 and the target in 2020 [43]

In the utilisation of renewable energy, wind energy, especially offshore wind energy, occupies a large proportion [43], [45]–[46]. This is because of the maturity of wind energy integration, and in comparison with the onshore wind energy, the intrinsic characteristics of offshore wind energy have more advantages, such as more wind blowing on the offshore sites, less noise and visual pollution [47]. For the integration of offshore wind energy, the use of MMC MTDC technology has advantages in three main aspects: 1) The offshore wind platform is always located far from the main power grid and massive power is generated from the offshore wind farms (OWFs), while HVDC has the advantages of bulk power submarine transmission over long distance [48]. 2) MMC VSC technology is capable of connecting weak AC networks, such as OWFs, rather than the integration using LCC technology which necessitates additional equipment such as STATCOM or SVC, to provide external commutation voltage

[49]. 3) The use of MTDC technology facilitates the integration of the wind farms at various locations and can interconnect the wind power with other generations and loads.

1.2 Literature Review

To provide an overview of the related research, an in-depth literature review is conducted in this section. MMCs are of state-of-the-art VSC type converters, while research on MMC MTDC systems such as the system start-up control, control and protection against AC and DC faults, has not been extensively investigated to date. Hence, a literature review will be conducted on VSC HVDC systems, while focusing on MMC MTDC, on 4 aspects: 1) simulation model and control of VSC HVDC systems; 2) start-up control of VSC HVDC systems; 3) control and protection of VSC HVDC under AC fault conditions; 4) control and protection of VSC HVDC under DC fault conditions.

1.2.1 Simulation and Control of VSC HVDC Systems

1.2.1.1 Simulation of VSC HVDC Systems

For VSC HVDC systems, due to the fast switching frequency of power electronic devices, the traditional simulation software which is mainly used for electromechanical transient simulations, such as PSS/E [50] in which the time-step is normally 10 ms, may not be able to explicitly present the system dynamics. However, the electromagnetic transient simulation software, such as the commonly used PSCAD/EMTDC [51] in which the time-step can be as small as 50 μs, can accurately reveal system dynamics.

For the state-of-the-art MMC [22], there are tens to hundreds of SMs in each MMC, while each SM has several semiconductor switches, which brings a computational challenge for

simulations and may significantly increase the simulation time [52] if no improvement is made on the method of simulation programme. In order to address the computational barrier, an efficient modelling approach, which drastically reduced the computational time while maintaining the accuracy, for simulations of MMC was proposed in [52]. However, the main limitation of [52] was that the proposed modelling approach was an equivalent modelling of MMC, which could not explicitly reveal the internal characteristics, such as the dynamics of charging and discharging of the SMs. Nevertheless, the proposed modelling approach would be useful for research in which the internal characteristics of the MMC are not the main focus. After that, other methods of modelling the MMC, which aimed at improving the simulation efficiency and accurately represented the system dynamics such as DC fault characteristics, were developed [53]–[57] with different types of MMC simulation models proposed. Two models amongst the proposed models, the average value model (AVM) and detailed switching model, have been widely used.

In the AVM, the dynamics of the SMs such as the charging and discharging process in the MMC, are not considered and it is assumed that the SM capacitor voltages are automatically balanced. Hence, the system performance, especially under dynamic conditions such as AC and DC faults, may not be explicitly revealed. In the detailed switching model, all the dynamic behaviour of the SMs is considered and the control strategy for balancing the SM capacitor voltages is required. Thus, the system performance can be well presented under both steady-state and dynamic conditions and more importantly, is close to reality. Nevertheless, the main problem of using the detailed switching model is the computational burden. With the efficient and enhanced modelling method of representing the characteristics of the MMC [53]–[57], the computational burden can be reduced. However, for the current MMC MTDC system, the computational challenge, especially for demonstrating the system performance

during a long period of time, such as the system performance under fault conditions, including the system recovery performance after fault isolation with associated control and protection actions, is markedly increased. The traditional simulation approach using offline simulation software can be utilised, but the simulation time may be considerable, which may hold up the research progress. The use of real-time simulators, such as the real-time digital simulator (RTDS) [58], which is specifically designed to perform electromagnetic transient simulations, can effectively solve this problem. Based on strong hardware and software, RTDS can achieve simulations and demonstrations of modern power systems in real-time. However, the main drawbacks of using RTDS are that the cost of the hardware, e.g. racks, processors, is considerable and the hardware-in-the-loop testing can only represent part of the real system. Hence, the selection of simulation platform should vary according to different purposes of research.

In [59]–[62], the performance of MMC MTDC systems under different dynamic conditions was investigated using RTDS. The operating characteristics of a 3-terminal MMC HVDC system under steady and dynamic conditions was studied in [59] and the effectiveness of the applied coordinated control strategies for the MTDC was verified. However, the investigated system was a simplest three-terminal MMC HVDC in radial structure without integration of renewable energy sources. In [60], a closed-loop testing of the droop control strategies of a 4-terminal MMC HVDC was implemented and the droop control strategies were validated. In [61], the operational and fault characteristics of an MMC MTDC system were investigated and the physical control system performance of the Nan'ao 3-terminal MMC HVDC project was evaluated. However, since the research was based on a real project, the MTDC system was in the simplest 3-terminal radial topology and only the master-slave control was considered. In [62], the performance of the CIGRE DC grids testing systems, including a 4-

terminal MMC HVDC and a full DC grid system with 9 MMCs, using the RTDS platform and offline simulation programme PSCAD was compared. The study results of the research conducted on an offshore MMC MTDC system in this thesis and the related publications were performed and verified on the RTDS. Since RTDS simulations have been verified by academic researchers [59]–[61] and industries [62]–[67], e.g. ABB [63], Siemens [64] and Alstom [65], and comparison studies have been conducted by researchers and RTDS teams [62]–[63], [66]–[67], the simulation results from RTDS are convincing.

1.2.1.2 Control of VSC HVDC Systems

For the control of VSC HVDC systems, the well-known *dq* decoupled control, also known as the vector control [68]–[69], is generally applied, so as to achieve independent control of active and reactive power. In the *dq* decoupled control, the *d*-axis generally applies constant DC voltage control, constant active power control or voltage droop control, which combines both DC voltage and active power control. The *q*-axis generally applies AC voltage control, reactive power control or a similar droop control, which combines both AC voltage and reactive power control. Figure 1-7 presents a control diagram of the *dq* decoupled control strategy.

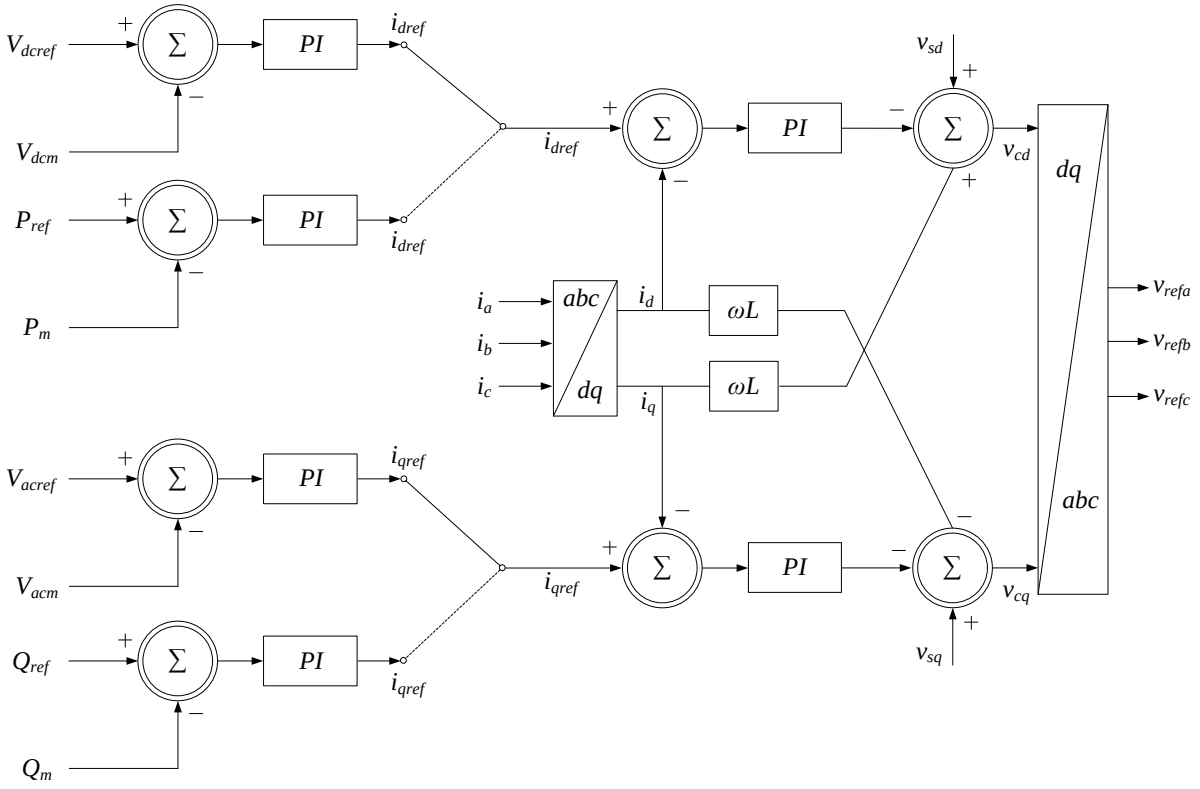


Figure 1-7 *dq* decoupled control

The use of *dq* decoupled control requires a nominal and stable AC voltage provided by the interconnected AC network. If the AC network has load or renewable energy sources, such as OWFs, which cannot provide such an AC voltage, the *dq* decoupled control cannot be applied. The AC voltage and frequency control [49], [70], V_{ac}-*f* control, is an alternative control strategy, which is widely used for integration of renewable energy, such as the OWF or load supply. Figure 1-8 presents a control diagram of V_{ac}-*f* control strategy.

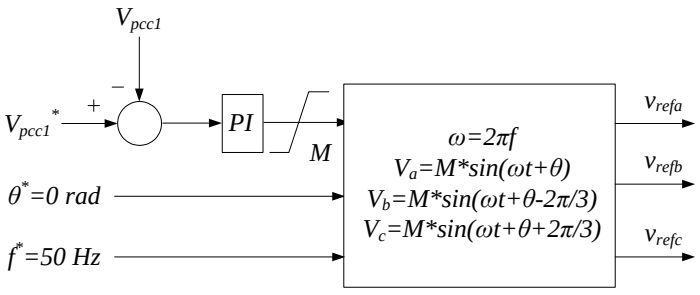


Figure 1-8 V_{ac}-*f* control

For VSC MTDC systems, 2 control paradigms, the master-slave control [33] and voltage droop control [38], [41], are generally used. For the master-slave control, one terminal is operated as the master terminal to maintain the DC voltage of the MTDC, while the other terminals are operated as slave terminals to control the active power. For the voltage droop control, the control of the DC voltage is shared among each terminal, which also has power sharing capability.

Due to the fact that the MMC is of VSC type, the aforementioned controls can be applied and are widely used in MMC HVDC systems. For the study system in [71], due to a 2-terminal MMC HVDC in which both terminals were connected with AC utility grids, the *dq* decoupled control was applied. One terminal controlled DC voltage control, while the other terminal acted as a power dispatcher. This control method has been generally used in 2-terminal including back-to-back systems. For the VSC HVDC investigated in [49] and [70], the terminal connected with the AC utility grid applied constant DC voltage control, while the other terminal was connected with the OWF, hence the V_{ac}-f control is applied to stabilise the magnitude and frequency of the terminal AC voltage at the point of common coupling (PCC) of the OWF.

In [33], [61], [72]–[73], master-slave control was applied for VSC MTDC systems. The advantages of master-slave control are that the control system design is relatively easy and for any change of active power in the DC grid only the master terminal is responsible for the power balancing, while there are few impacts on the slave terminals. However, if a fault occurs at the master terminal, it may lead to the collapse of the DC grid voltage. In addition, if the fault is permanent, the master terminal cannot resume after the fault isolation. The recovery of the unfaulted terminal necessitates one of the slave terminals to switch its control

mode to take over the DC voltage control and then the remaining unfaulted terminals can resume.

In [38], [40]–[41], [59], [62], [74], voltage droop control was applied in the VSC MTDC systems. The advantage of droop control is that the power balancing burden is not put on one terminal, since not only one terminal has power sharing capability. Moreover, since the DC voltage control is shared among each terminal, each terminal is capable of supporting the DC voltage and the system can resume in an easy and efficient manner after the fault isolation. However, its drawback is that the design of the control system is relatively complex in consideration of the droop characteristics. In addition, any change of active power in the DC grid will have an impact on the terminals with droop control, which may cause problems such as current over limit or multiple operating points [75], if the controller is not properly designed.

The MMC MTDC model used in this thesis applies master-slave control, while the proposed control strategies, such as the start-up control, control and protection strategies against AC and DC fault conditions, are applicable for MMC MTDC systems with either master-slave control or droop control.

For the MMCs, apart from the basic control of the traditional VSCs, some additional control is also necessary, such as the SM capacitor voltage balancing control [71], [76], circulating current suppression control [77] and modulation of the gate signals for each SM [78]–[79]. However, since these topics have been comprehensively investigated and are not the focus of this thesis, literature review is not conducted in detail on these topics.

1.2.2 Start-Up Control of VSC HVDC Systems

Every system must experience the start-up process before reaching the steady state. For VSC HVDC systems, it is important to achieve the start-up of the systems in a stable and smooth manner with small voltage spikes and current surges. The start-up control of VSC HVDC systems is influenced by many factors, such as different topologies of the converters, the characteristics of the interconnected AC networks, and the number of terminals of the whole network.

For the traditional 2-level VSC HVDC system, the IGBTs in the converter station are connected in series and only the converter DC-side has DC capacitors. During the start-up process, only the DC-side capacitors and the DC network needs to be pre-charged. Hence, the self-start-up of the system is not complex. Most research focused on the control of the 2-level VSC HVDC for the facilitation of the start-up of other systems rather than the start-up control of the system itself. In [80], the use of a 2-level VSC HVDC for the start-up of the conventional LCC-HVDC whose receiving side was a passive network was proposed. The control strategy of the VSC HVDC for providing the commutation voltage for the start-up of LCC was described. However, detailed start-up sequences of the system were not comprehensively introduced. In [81], the control of a 2-level VSC HVDC to achieve "soft start-up" of switching on a long no-load line in power systems to reduce the switching surges was investigated. According to three comparative studies, the system using "soft start-up" approach significantly reduced the switching surge. However, the implementation of the "soft start-up control" was not clearly explained in the simulation case. In [82], the black-start function of 2-level VSC HVDC as a source for AC grids was investigated and comparisons of the start-up performance were made between using the VSC HVDC and the traditional black start units. However, the study results were mostly based on simulations with little mathematical analysis.

For the MMC HVDC system, the converter topology is more complex than that of the 2-level VSC HVDC. There are numerous SMs in the converter station and each SM has its energy storage capacitor. During the start-up process, not only the DC network needs to be pre-charged, but the capacitors in all the SMs also need to be pre-charged. In addition, regarding the characteristics of the interconnected AC networks, i.e. active network or passive network, the pre-charging characteristics of the SM capacitors are different. Hence, the start-up control of an MMC HVDC system is more complex than that of the 2-level VSC HVDC. Furthermore, if an MMC MTDC system is considered, the start-up control sequence also needs to be taken into account and an effective control sequence becomes important.

A start-up control scheme for the MMC was proposed in [83]. The control scheme was based on the control of an auxiliary voltage source, which was connected at the MMC DC-side. However, it is generally expected to start a system without auxiliary sources, which saves space and costs. In [84], a 2-stage start-up scheme for MMC HVDC was proposed, including the calculation of the limiting resistance, the setting of the rising slope of DC voltage and the reference setting of reactive power. In [85], a start-up scheme with a 2-stage pre-charging process for MMC was proposed. Although the proposed charging scheme seemed to achieve the pre-charging of SM capacitor voltages to the rated value without auxiliary DC source, it had two main limitations. At the first pre-charging stage, the DC voltage was assumed to be the rated value and the pre-charging of the SM capacitors was from the DC side. Under this assumption, the proposed scheme was only valid for the MMC under inverter operations. At the second pre-charging stage, the proposed scheme was that the SM capacitor voltages were pre-charged to the rated value when the SMs were deblocked. However, the main objective of the start-up control of an MMC is to pre-charge the SM capacitors to the rated value before they are deblocked. In [86], the dynamics of the SMs in the MMC during the pre-charging

process was analysed and an optimised modulation algorithm was proposed for reducing the charging current when deblocking the MMC. Theoretically, an MMC can be deblocked at zero voltage difference and the current surges under this condition are the smallest. However, the control scheme proposed in [86] did not achieve zero voltage difference when deblocking the MMC. The start-up schemes proposed above were all based on 2-terminal MMC HVDC systems. In [87], a 3-terminal MMC HVDC system based on a real application was investigated and the control procedures of starting the system were proposed in detail. However, these procedures were obtained as a conceptual approach, which was based on the analysis at systematic level. There was no analysis on the dynamics of the SMs in the MMC and no comprehensive simulation results. Hence, the start-up control including the start-up sequence of MMC MTDC systems deserves our study and exploration.

1.2.3 Control and Protection of VSC HVDC under AC Fault Conditions

In electrical power transmission systems, there has been a long history of research on control and protection against AC faults [88]–[89]. This technology has reached a high maturity with comprehensive control and protection schemes being proposed for different fault conditions. Regarding VSC HVDC systems, research focus has been predominantly on control and protection against DC faults. This is because unlike the LCC HVDC, DC fault currents cannot be regulated. However, control and protection against AC faults in VSC HVDC systems is not simple and has its complexity. The complexity is mainly caused by the variations of 1) fault types; 2) fault location; 3) system configuration.

1) Fault types: AC faults have two different types, symmetric faults and asymmetric faults. The symmetric faults include three-phase short-circuit faults, three-phase to ground faults. The asymmetric faults include single-phase to ground faults, two-phase short-circuit faults

and two-phase to ground faults. Control and protection strategies against different types of faults are different, while each fault can be a transient or a permanent one, which further increases the complexity of control and protection schemes.

2) Fault location: Regarding AC faults occurring at different terminals, the system will have different fault characteristics since the VSCs at different terminals have different control modes. Furthermore, for AC faults occurring at one terminal, fault locations may be different. Some may locate within the protection range of the AC circuit breakers, while some may locate beyond the protection range of the nearby AC circuit breakers. Hence, the associated control and protection strategies will be different depending on the fault location.

3) System configuration: For multi-terminal VSC HVDC systems, control and protection strategies will become more complex than those of the 2-terminal systems. This is because the fault detection, location and isolation become more complex with the increased number of terminals and variations of control characteristics of the VSCs. In addition, after fault isolation, the recovery control of the unfaulted terminals needs to be considered, while different recovery strategies vary with different fault locations.

Therefore, control and protection against AC faults in VSC HVDC systems deserves our study and exploitation.

Previous literature mainly focused on research of transient AC fault conditions. In [35], the fault characteristics of an MMC HVDC system under AC faults at different locations were investigated and the differences of the characteristics due to different control modes of the converters were identified. However, the associated control and protection strategy was not comprehensively investigated.

In [90]–[93], VSC-HVDC systems under asymmetrical AC fault conditions were investigated. In [90], the differences of the fault characteristics of an MMC HVDC and a 2-level VSC HVDC under a same single-phase to ground AC fault were analysed and demonstrated. It was discovered that due to the advantages of the MMC topology, the fault ride-through (FRT) capability of MMC HVDC is stronger than that of the 2-level VSC HVDC. In addition, the potential problem of insulation due to the voltage rise after asymmetric fault was investigated with a proposal on the requirement of the protection system. In [91] a method, which was based on estimation of positive and negative sequence of virtual flux components, being able to prevent the power oscillations in the DC network, while maintaining the currents within the limited rating under unbalanced AC fault conditions was proposed. Thus, unexpected blocking of the converter and tripping of the AC system could be effectively prevented using this method. For MMC-HVDC system under asymmetrical faults, [92] reported that there would be second-order harmonic in the DC voltage, even if the negative-sequence current controller was employed, because of the zero-sequence voltages in the three-phase units. A DC voltage ripple suppressing controller was proposed to eliminate the second-order harmonic in the DC voltage by compensating the zero-sequence voltages. However, since the arm voltage measurements were needed, some additional hardware and cost were introduced. In [93], the fault characteristics of 3 different single-line-to-ground fault conditions in an MMC-HVDC system were investigated. A double-line frequency DC voltage ripple suppression control was proposed. The fault-tolerant capability of the system could be enhanced using this controller with no extra hardware needed. A control strategy was proposed in [94], which could allow the VSC HVDC to ride through different AC faults, including both symmetric and asymmetric faults, with minimum voltage spikes and current surges. This could effectively mitigate the voltage rise in the DC grid, which contributed to

the potentiality of eliminating the need for DC choppers. In [95], a hybrid multilevel VSC with AC-side cascaded H-bridge cells was proposed, which could improve the system AC FRT capability. However, the main drawback of this method was that the introduction of the additional cascaded H-bridge cells incurred extra hardware and associated cost.

In [96]–[99], wind farm integrated VSC HVDC systems under AC faults were investigated. In [96], the performance of a 3-terminal VSC HVDC grid with a large OWF under two-phase and three-phase short-circuit faults in the collection grid was studied. With the action of the DC-chopper, the wind turbines could operate stably under fault conditions. However, the faulted section should be fast located and disconnected to assure the unfaulted part remaining in stable operation after the fault. In [97], a new control approach for FRT of wind farm connected VSC-HVDC transmission was proposed. The proposed approach allowed a fast power reduction by initiating a controlled voltage drop in the wind farm grid during AC faults, which avoided overvoltage in the DC grid and saved the cost of DC chopper circuits. In [98], a new system configuration for VSC HVDC was proposed and could allow smooth power transfer from offshore wind power plant under symmetrical and asymmetrical faults in AC power networks. In addition, a transient management scheme with positive and negative sequence controllers was developed. The controller was able to handle various AC faults and mitigate DC voltage ripples under asymmetrical faults. In [99], communication-free control strategies were proposed for MTDC grids. The proposed approach could mitigate the DC voltage rise effect during AC faults and could avoid the use of chopper resistors in the MTDC grid. However, small overcurrents could be observed in the VSC, which should be carefully considered at the design stage.

The attention of the aforementioned literature focused on control and protection against

transient AC faults, while there has been little research focusing on control and protection against permanent AC fault conditions. In [100]–[101], the dynamic behaviour of a VSC MTDC system under a permanent AC fault was investigated. However, research focus was mainly put on the system fault characteristics and the impact of the fault on the system AC and DC side. The associated control and protection means were not investigated. For permanent AC faults, since they cannot be cleared within a short period, associated control and protection action, such as blocking of the converter station and tripping of the AC circuit breakers, may be necessary. Normally, if the fault occurs within the protection range of AC circuit breakers, the tripping of the nearby AC circuit breakers can achieve the fault isolation. However, if the fault occurs close to the converter station that is beyond the protection range of the nearby AC circuit breakers, a special control and protection strategy may be required. Hence, comprehensive research on control and protection of VSC HVDC under permanent AC fault conditions deserves our attention and further investigation.

1.2.4 Control and Protection of VSC HVDC under DC Fault Conditions

In VSC HVDC systems, the study and exploitation of control and protection against DC faults has always been research interest in the last several decades. This is because of the following reasons: 1) The DC fault characteristics have large differences with those of the traditional AC faults, which brings challenges to the fault detection and fault location. 2) DC fault currents will rise rapidly and dramatically after the fault occurs. In comparison with that of AC faults, the impact of DC faults on the VSC HVDC system is considered to be more considerable. 3) Unlike the LCC, the VSC is not capable of controlling the DC fault current. In addition, the ratings of the IGBTs in the VSC are generally much lower than those of the thyristors in the LCC. Hence, VSC HVDC is considered to be vulnerable to DC faults; 4)

Unlike AC fault currents, DC fault currents do not have stable zero-crossing points, which increases the difficulty and challenge on the design of DC circuit breakers. 5) DC fault isolation cannot be achieved by just blocking the VSC, since the AC side can still contribute to DC fault current through the diodes in the VSC, necessitating tripping of the AC circuit breakers at the adjacent terminals. 6) For VSC HVDC, particularly VSC MTDC systems, fast and stable recovery of the system after the fault isolation is important.

Previous research of DC faults in VSC HVDC systems mainly focuses on: 1) fault characteristics; 2) fault detection and location; 3) fault isolation.

In [102]–[106], the fault characteristics of VSC HVDC systems under DC fault conditions were studied. DC line-to-ground fault would cause unbalanced DC voltage was identified in [102]. Solutions, such as grounding with large resistance, to avoid the voltage unbalance were proposed. DC line-to-line fault would result in fast discharging of DC-side capacitors and DC fault currents contributed from the AC side were also demonstrated in [102]. Hence, it is necessary to trip AC circuit breakers to isolate the fault. The research of [103] indicated that the configuration of transformers and the grounding of the DC-side capacitors had impact on the system fault behaviour under DC line-to-ground fault. The impact of 2 grounding schemes, transformer ungrounded/DC-side grounded and transformer grounded/DC-side ungrounded on the system dynamic behaviour after a line-to-ground fault was discussed in [103] and it is identified that the potential earth loop might lead to overcurrent flowing through the VSC causing system oscillations. In [104], the transient performance of a VSC MTDC with wind farm integration under short-circuit fault and cable ground faults was investigated. A system protection design with relay coordination method was proposed with a diode clamping method, which was effective when DC circuit breakers were not economically feasible. In

[105], the protection scheme of a meshed 5-terminal VSC HVDC grid under fault events was investigated. The overcurrent caused by a fault was identified to be significant. In addition, the performance of the differential current protection approach for a faulted cable and a healthy cable was demonstrated and compared. In [106], the impact of different grounding schemes of meshed HVDC grids on the system fault behaviour was investigated. Different grounding schemes would determine the system with low or high impedance grounded and have a significant impact on the system fault characteristics. Asymmetric grid configurations with low impedance grounded and symmetric grid configurations with high impedance grounded were suggested, respectively.

For VSC HVDC, especially VSC MTDC systems, fast and accurate detection and location of DC fault is important. In [107], a fast and reliable technique for fault detection and location, which was based on the voltage and current characteristics of each VSC following a fault, was proposed. However, this technique required the communications among the VSCs. In [108], a handshaking method was proposed for locating and isolating the faulted DC line without the need of telecommunication. Although the proposed method could locate a fault on a line of the meshed DC grid, it could not specify the exact fault location due to the fact that the proposed method was only based on the characteristics of the magnitude and direction of the fault current. The determination of the exact fault location is essential for a permanent fault condition, e.g. a cable fault, which requires repairs or replacements of the faulted section. In [109], a protection algorithm which was based on wavelet analysis, for locating the DC fault was proposed. This method realised the fault location by local measurement without the need of communication among the VSCs and could achieve fast and reliable cable fault detection. The simulation results demonstrated the proposed method could detect the fault within 1 ms. In [110], a DC fault detection and location technique, which combined the wavelet analysis

and travelling wave method was proposed. In this method, the wavelet analysis was mainly used for detecting the fault type and locating the faulted line, while the travelling wave method could further precisely locate the fault.

The DC fault isolation in VSC HVDC systems can be achieved either by the traditional method of blocking the VSC and tripping the AC circuit breakers or using advanced techniques, such as the DC circuit breakers [111], full-bridge/hybrid MMCs [28]–[29], DC-DC converters [37] and others. Previous literature was mainly focused on the research of the latter techniques.

The study in [100] demonstrated that a permanent DC fault in a VSC MTDC might cause system black outs, which indicated the importance of prompt protection actions. The fault isolation and system recovery proposed in [100] were conducted through the action of the DC circuit breaker and it was found that effective fault isolation and system recovery could be achieved when the DC circuit breakers were located in an appropriate distributed way. The proposed scheme could be applied for offshore VSC MTDC networks. However, this scheme was established based on the concept and simulations of using DC circuit breakers in which the detailed circuit topology was not analysed. In [112], a circuit topology of the DC circuit breaker for VSC HVDC was proposed. With multiple semiconductors connected in series, this DC circuit breaker could achieve high blocking voltage and by using a diode, which provided a bypassing path for the fault current, the proposed circuit could realise surge voltage reduction. Although high-speed DC circuit breakers have been extensively explored by all major HVDC equipment suppliers [26] and different prototypes of hybrid DC circuit breakers were announced to be developed [111], [113] which were considered to be huge breakthrough, these DC circuit breaker technologies have mainly been demonstrated on the

laboratory voltage scale and its expense could be considerable.

The full-bridge MMC has DC fault current blocking and control capability [28]–[29], [114], since the polarity of the SM output voltages can be flexibly adjusted. However, the drawbacks of the full-bridge MMC, in comparison with the half-bridge MMC, are the doubled number of switching devices and higher losses. In order to address this concern, a hybrid MMC topology, AAC, in which the 2-level IGBT modules and full-bridge SMs were series connected on each arm, was proposed in [13] and [31]. This topology also has the DC fault blocking capability, while it reduced the number of semiconductor devices used in the full-bridge MMC. Based on the concept of AAC, [115] demonstrated that the AAC could ride through the DC fault without the necessity of tripping the AC circuit breakers and thus reduced the system recovery period. The STATCOM operation mode of the AAC, which enhanced the stability of the AC network during the fault period, was also presented [115]. Although the number of switching devices in the AAC becomes smaller compared with the full-bridge MMC, in comparison with the half-bridge MMC, the AAC topology still requires extra switching devices due to topological effects associated with the converter configuration.

The use of DC-DC converters to isolate the DC fault was proposed in [37], [116]. In [37], a high-power bi-directional DC-DC converter topology was proposed. The DC fault isolation could be achieved by controlling the DC-DC converter, while the operation of the remaining DC lines was not affected. A DC-DC converter with half- and full-bridge SM, which acted as a DC chopper, for isolating and clearing the faulted line, was proposed in [116]. The proposed DC-DC converter could suppress the overcurrent under DC faults and reduce the overvoltage under AC faults. The main drawback of DC-DC converters, which limits the applications, is the losses and considerable cost.

In the advanced techniques for DC fault isolation, there are some other approaches apart from the use and control of DC circuit breakers, full-bridge/hybrid MMCs, and DC-DC converters. In [117], a VSC-based hybrid converter topology, which was formed by AC-DC and high-frequency DC-DC modules, was proposed. It could achieve the DC fault protection without the DC circuit breakers. The fault operation and system recovery using the proposed topology were validated on the PSCAD software and hardware-in-the-loop testing using RTDS. In [118], a buck-boost inverter-based HVDC system, which could block the current flowing from the AC-side to the DC-side under DC faults by simply disabling the gate signals, was proposed. The advantages on the DC fault protection were demonstrated in the comparison with the traditional VSC HVDC system. However, its drawbacks were the requirement of high ratings of the semiconductors, increased number of semiconductors and high losses. In [119], a protection scheme for handling transient faults on DC overhead lines was proposed. The diode freewheeling effect could be eliminated by employing double thyrisitor switches on the half-bridge MMC and thus the DC fault current can decay to zero. The proposed protection scheme could fast clear faults and recover the power transmission without tripping the AC circuit breakers. However, this protection scheme could not ensure fast blocking of the fault current and was only applicable for non-permanent fault conditions on DC overhead lines.

Previous reviewed literature mainly focused on control and protection against DC faults at the detection, location and isolation phases using advanced protection approaches, while there has not been much research that investigated the system recovery control after the fault isolation using the traditional control approach by tripping the AC circuit breakers. Before the advanced technologies become commercially available and viable, it would be meaningful to investigate control and protection strategy with traditional control approach, particularly the

system recovery after the fault isolation for an MMC MTDC system.

1.3 Research Objectives and Contributions

The test system is an MMC MTDC system with an OWF. The research focus is mainly on the system and converter level control of this system instead of the detailed modelling and valve level control of the MMC. The objective is to improve the system dynamic performance with fewer voltage spikes and current surges under three conditions: 1) start-up; 2) AC fault; 3) DC fault, by appropriate control sequences.

1.3.1 Start-Up Control

In principle, with effective start-up control, an MMC can be deblocked with minumum voltage difference on the SMs during the start-up process, regardless of whether the MMC is connected with an active or passive AC network. However, the minimum voltage difference at deblocking the MMCs was not achieved based on the control methods proposed in the previous literature, while the minimum voltage difference, especially zero voltage difference, will lead to minimum voltage spikes and current surges when deblocking the MMCs. In addition, there have been few proposals regarding the start-up control of offshore integrated MMC MTDC systems, while the start-up control sequence of each terminal has a significant impact on the system start-up performance.

This thesis will investigate the start-up control of an offshore integrated MMC MTDC system. Firstly, mathematical models of the MMCs before and after the deblocking action will be analysed and established during the start-up process. According to the analysis of the mathematical model, a hierarchical start-up control scheme will be proposed for the MMC

with active AC networks, while a reduced DC voltage control scheme will be proposed for the OWF connected MMC. A comprehensive start-up control scheme will be formed for the offshore MMC MTDC system by combining both schemes. The proposed start-up control scheme can achieve minimum voltage difference on SMs when deblocking the MMCs and with an appropriate system parameter design, zero voltage difference may be realised.

1.3.2 Control and Protection against AC Faults

Previous literature has mainly focused on control and protection strategy of VSC HVDC systems under transient AC fault conditions, particularly the system fault ride-through capability. However, for permanent AC fault conditions in which the fault occurs beyond the protection range of the nearby AC circuit breakers, there has been less research. Moreover, for MTDC systems, the system recovery control needs to be considered for resuming the unfaulted terminals after the fault isolation.

This thesis will study and explore control and protection of the offshore MMC MTDC system under permanent AC fault conditions, particularly when the fault occurs at the MMC AC-side, which is beyond the protection range of the nearby AC circuit breakers. Apart from that, there has been little attention on such a fault condition that the fault occurs at the MMC AC-side, while the faulted-side MMC experiences different conditions of blocking failure. This thesis will investigate such a fault condition. Two different conditions, emergency condition and non-emergency condition, will be categorised according to the analysis of the blocking failure conditions, and the corresponding control and protection strategy will be proposed for each condition.

1.3.3 Control and Protection against DC Faults

Although there has been extensive research on control and protection against DC fault conditions of VSC HVDC, research effort was mainly put on the advanced protection techniques such as the design and control of DC circuit breakers, and there have been few publications regarding the traditional protection method of using AC circuit breakers on the MMC MTDC systems. The advanced protection techniques could have potential applications in the future. However, before they become commercially available and viable, some operational schemes should be in place. Although the traditional protection method requires the tripping of the AC circuit breakers at all adjacent terminals, it is an economical and feasible solution.

This thesis will investigate control and protection of the offshore MMC MTDC system using the traditional protection method under DC fault conditions, particularly the system recovery control after the fault isolation. The recovery control, including when to start the recovery control, the recovery control at each terminal and the recovery sequence among difference terminals, has a significant impact on the system performance. In addition, the recovery control may vary according to the fault location. This thesis will investigate the aforementioned aspects and propose control and protection schemes under different DC fault conditions. Simulation results on the RTDS will be used to evaluate the effectiveness of the proposed schemes.

1.4 Thesis Outline

The thesis consists of 7 chapters and the relationship of the remaining chapters is that: **Chapter 2** gives an overall picture and the fundamental information of the offshore MMC MTDC test system for the following chapters. From **Chapter 3** to **Chapter 6**, each chapter

investigates the performance of the test system under a specific type of conditions. **Chapter 7** concludes the thesis and suggests future work.

An outline of each chapter is described below.

Chapter 2 provides an introduction to the offshore MMC MTDC test system, including the system configuration; the structure, control mode and reference settings of the MMC; the structure and control of the OWF.

Chapter 3 studies the system performance under steady-state condition, the system dynamic performance under a transition from one steady-state to another steady-state and evaluates the system power balancing and power flow reversal capabilities.

Chapter 4 analyses the system start-up characteristics and establishes corresponding mathematical models. For the onshore terminals, a hierarchical start-up control is proposed. For the offshore terminal, a start-up scheme with reduced DC voltage control is proposed. A combination of the start-up control of both the onshore and offshore terminals forms a comprehensive start-up control sequence.

Chapter 5 studies the system fault characteristics under a permanent three-phase to ground fault at different locations. The corresponding control and protection strategy against the fault is proposed according to the fault characteristics. Some emergency conditions and potential risks are identified with special control and protection strategy proposed.

Chapter 6 studies the system fault characteristics under a permanent DC pole-to-pole fault at different locations. The corresponding control and protection scheme at the fault

isolation phase is presented according to the fault characteristics. Control and protection scheme at the system recovery phase is analysed and proposed with a DARC scheme proposed. A comprehensive control and protection sequence is proposed by synthesising control and protection scheme at every phase.

Chapter 7 draws conclusions of the thesis. Based on the research outcomes, some future work that deserves further research and study is suggested.

CHAPTER 2 CONFIGURATION, STRUCTURE AND CONTROL OF THE MMC MTDC SYSTEM WITH AN OWF

Before discussing the steady-state performance, start-up control, control and protection against faults of the test system, the system configuration, detailed structure and control mode applied need to be introduced. This chapter gives an overall picture and the fundamental information of the test system for the following chapters.

2.1 Introduction

In this chapter, the system configuration is presented. Then two key components, the MMC and OWF, are introduced respectively. For the MMC, its structure and control mode are described. For the OWF, its structure and basic control strategy are introduced.

2.2 System Configuration

A single-line schematic representation of the test system configuration is shown in Figure 2-1.

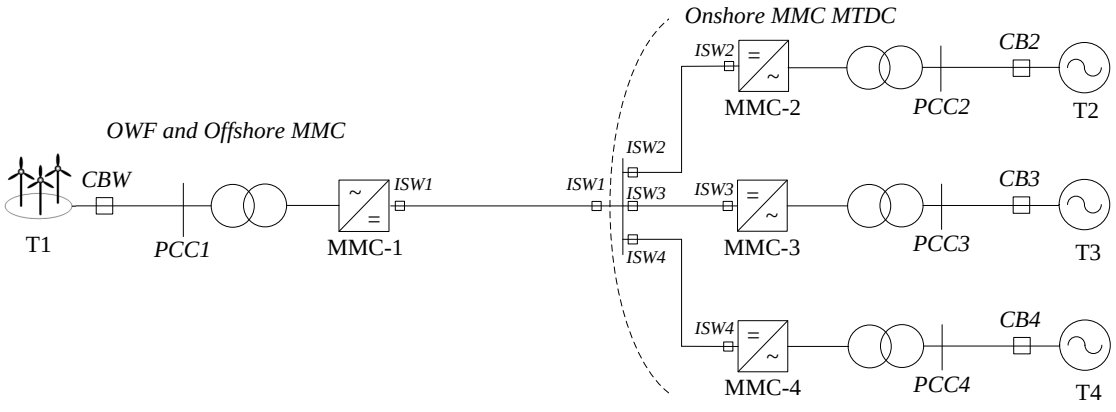


Figure 2-1 Configuration of the OWF integrated 4-terminal MMC HVDC system

This is a 4-terminal MMC HVDC system where the OWF is integrated at T1. In Figure 2-1, *Tn* (*n* = 1,…,4) denotes each terminal of the MTDC system; *CBW* denotes the AC circuit breaker at the OWF terminal; *CBn* (*n* = 2,…,4) denotes the AC circuit breaker at each terminal; *PCCn* (*n* = 1,…,4) denotes the point of common coupling at each terminal; MMC-*n* (*n* = 1,…,4) denotes the MMC at each terminal; DC *ISWn* (*n* = 1,…,4) denotes the DC isolation switch at each terminal.

On the MMC DC side, the 4-terminal system is radially interconnected. The DC network uses a cable model where the length of each DC Cable is 100 km. Each DC cable has DC *ISW*s equipped at both ends. The DC *ISW*s are mainly used for the isolation of the faulted section line after the initial control and protection action against a fault. However, compared with the DC circuit breaker, the DC *ISW*s can only be opened when its current becomes sufficiently small. On the MMC AC side, MMC-1 is connected with the OWF through a three-phase transformer, while the other three MMCs are connected to AC utility grids via transformers. The system parameters can be found in Appendix A.

The structure of an MMC and the control mode of the MMC at each terminal will be described in Section 2.3 and the structure and basic control strategy of the OWF will be introduced in Section 2.4.

2.3 MMCs

The MMC is one member of the VSC family. The most basic topology of an MMC is the half-bridge MMC [12], [22]. There are also advanced variations of the MMC topologies, such as the full-bridge [28]–[29] and hybrid MMC [28]–[29], [31]–[32]. The MMCs investigated in this thesis are the basic half-bridge MMCs. The control of an MMC can be divided into 3

levels: system level, converter level and valve level, as illustrated in Figure 2-2.

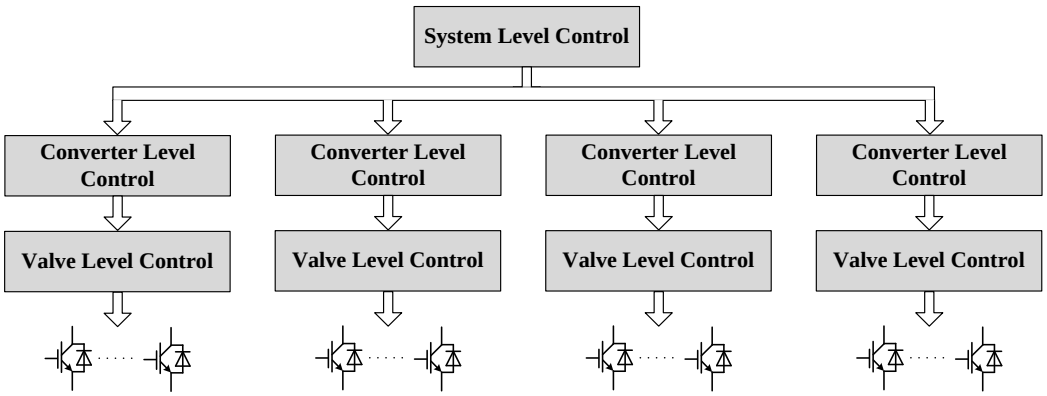


Figure 2-2 System level, converter level and valve level control of an MMC

The control modes of the conventional 2-level VSC and the MMC at the system and converter level are similar. However, the MMC structure and its operating mode at the valve level are different with the 2-level VSC. In the following sub-sections, the MMC structure will be presented and the operating mode at the valve level, the control modes at the converter level and the reference settings at the system level will be described.

2.3.1 Structure

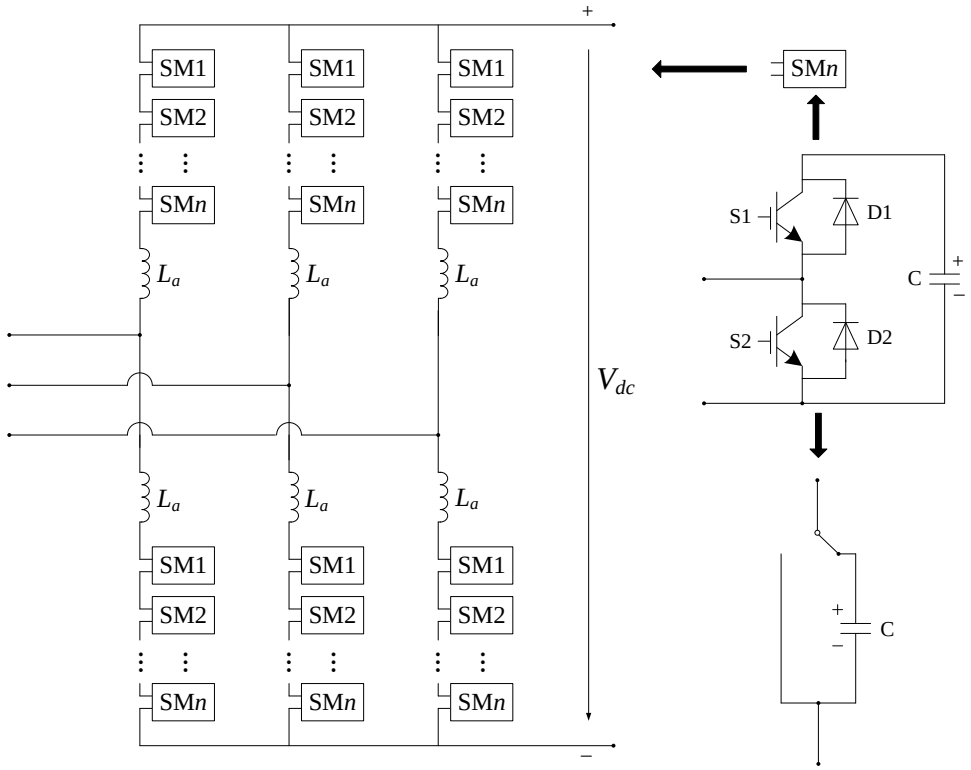


Figure 2-3 Structure of an MMC

The structure of a half-bridge MMC is shown in Figure 2-3. The basic structure of an MMC is a 3-phase, 6-arm bridge, which is the same as a 2-level VSC. However, in the 2-level VSC, each arm has numerous IGBTs connected in series as shown in Figure 2-4.

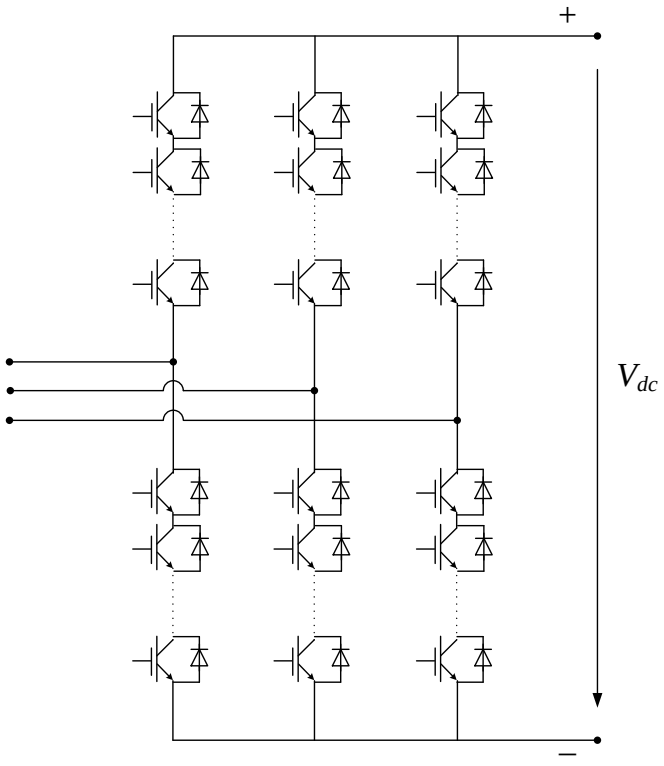


Figure 2-4 Structure of a 2-level VSC

The operation principle of the 2-level VSC requires synchronous turn-on and turn-off of the series-connected IGBTs, hence the modulated voltage at the VSC AC-side is 2-level square wave. In the MMC, each converter arm comprises an arm inductor and numerous SMs connected in series. The arm inductor is designed for two main reasons [71], [77]: 1) to provide current control and limit the circulating current within the arm; 2) to limit fault currents. Each SM comprises two IGBTs and one energy storage capacitor as shown in Figure 2-4.

2.3.2 Operating Mode at Valve Level

This section describes the operating mode of the MMC at the valve level, i.e. the switching mode of its SMs. Under normal operating condition, an SM has two switching modes:

- Mode 1: S1 is switched-on and S2 is switched-off. Under this mode, the SM is switched-on and has the following features:
    - The SM capacitor is switched into the arm circuit;
    - The arm current flows through the capacitor and either charges or discharges it depending on the current direction;
    - The terminal voltage of the SM equals to the capacitor voltage, v_c.
- Mode 2: S1 is switched-off and S2 is switched-on. Under this mode, the SM is switched-off and has the following features:
    - The SM capacitor is bypassed from the arm circuit;
    - The arm current does not flow through the capacitor;
    - The terminal voltage of the SM equals to 0.

Since the terminal voltage of the SM can be regulated, each SM becomes a controllable voltage source and the series-connected SMs form an equivalent AC voltage source [21]. The equivalent circuit diagram of an MMC is depicted in Figure 2-5. Each SM can generate and control one voltage level, hence the modulated voltage at the MMC AC side is a staircase wave which is closer to sinusoid with fewer harmonic proportions than a 2-level square wave. Figure 2-6 shows the modulation of a 2-level square wave and a staircase wave. It is generally defined that the number of level of an MMC is $n+1$ if the number of SMs on each arm is n.

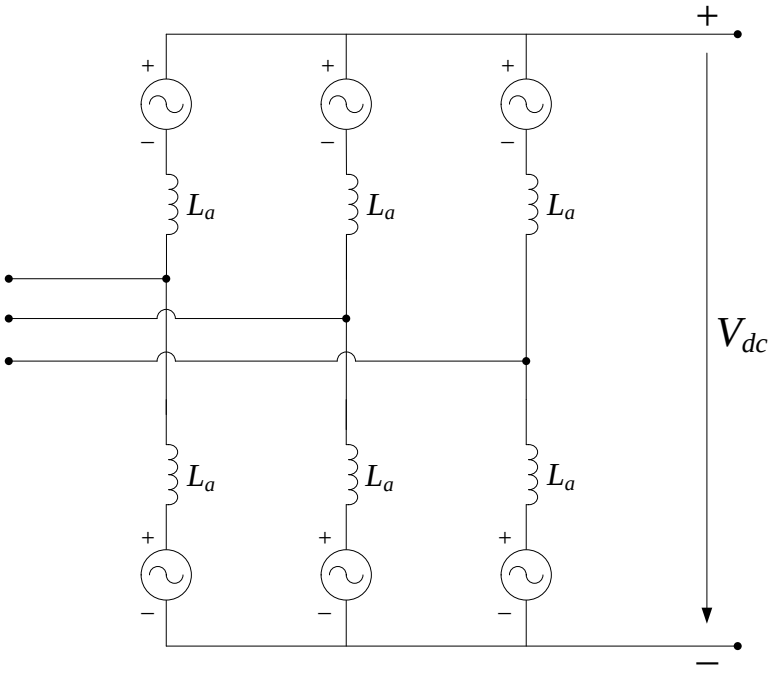


Figure 2-5 Equivalent circuit diagram of an MMC

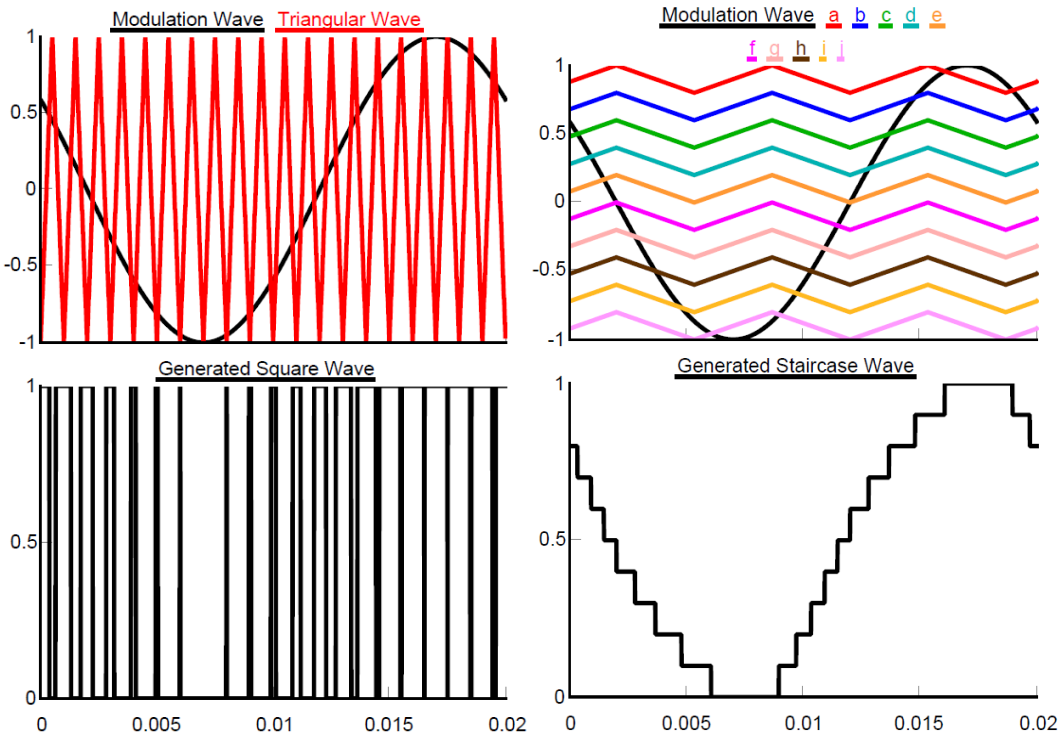


Figure 2-6 (a) Modulation of a 2-level square wave; (b) Modulation of a staircase wave

When the number of level of the MMC is increased to a certain degree, with appropriate control applied, the performance of the output voltage will be improved with potentiality of removing the AC filters, which largely reduces the cost and the footprint of the system. Since there are tens or hundreds of SMs per converter arm, the nearest level modulation (NLM) technique [78] is generally applied to dertermine the number of SMs to be inserted (ON) and bypassed (OFF). Figure 2-7 presents a block diagram of the NLM in the RTDS.

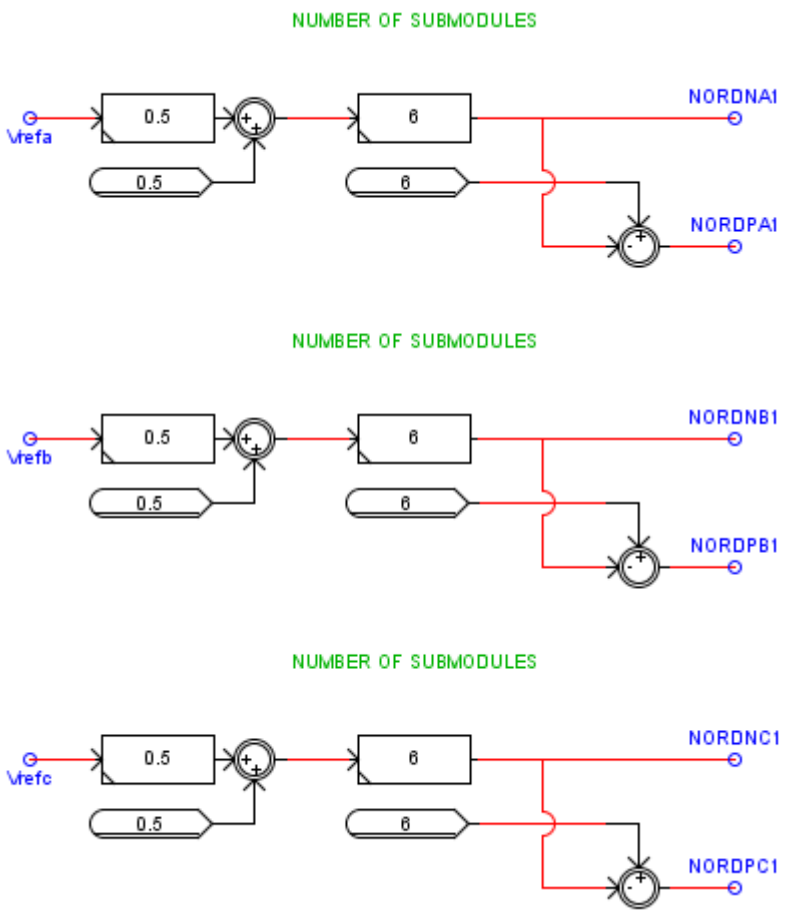


Figure 2-7 Control diagram of NLM in the RTDS

In Figure 2-7, V_{refa}, V_{refb}, V_{refc} are the three-phase reference voltages at the MMC AC-side and are the outputs of the converter level control. The generated reference voltages are controlled to determine the number of ON and OFF SMs on the upper and lower arms of the

MMC. *NORDijk* (*i* = *P*, *N*; *j* = *A*, *B*, *C*; *k* = 1,…,4) represents the number of ON SMs on the upper arm (*i* = *P*) or lower arm (*i* = *N*) of Phase *j* of MMC-*n* and can be calculated as:

$$NORD_{Pjk} = N \cdot \left(\frac{1}{2} - \frac{1}{2} V_{refj} \right) \tag{2.1}$$

$$NORD_{Njk} = N \cdot \left(\frac{1}{2} + \frac{1}{2} V_{refj} \right) \tag{2.2}$$

No matter what switching mode a SM applies, the arm current can bi-directionally flow through the SM under normal operating condition. Therefore, different with that of the IGBTs in the 2-level VSC, its operating principle does not require synchronous operation on the series-connected SMs. This feature largely reduces the difficulty on the design and manufacturing of the MMC and increases its availability and efficiency [22], since the realisation of synchronous operation of the series-connected IGBTs of the conventional 2-level VSC has always been a challenge and may lead to large power losses if an error exists in the synchronicity. Moreover, since the MMC AC side voltage generated by the MMC is a staircase wave and each SM is operated independently of the others, its switching frequency is largely reduced, which contributes to lower switching losses.

In the MMC, apart from the generation of the desired modulation wave, the operating principle requires the balancing of the capacitor voltages of the series-connected SMs [71], [76]. Therefore, a capacitor balancing strategy is needed. In this thesis, the sorting method is applied for the capacitor voltage balancing, that is:

- When the arm current is to charge the SM capacitors, the SM capacitors monitored with relatively lower voltages are charged first;
- When the arm current is to discharge the SM capacitors, the SM capacitors monitored

with relatively higher voltages are discharged first.

Figure 2-8 presents a block diagram of the capacitor balancing control of the upper arm of Phase A of MMC-1 in the RTDS.

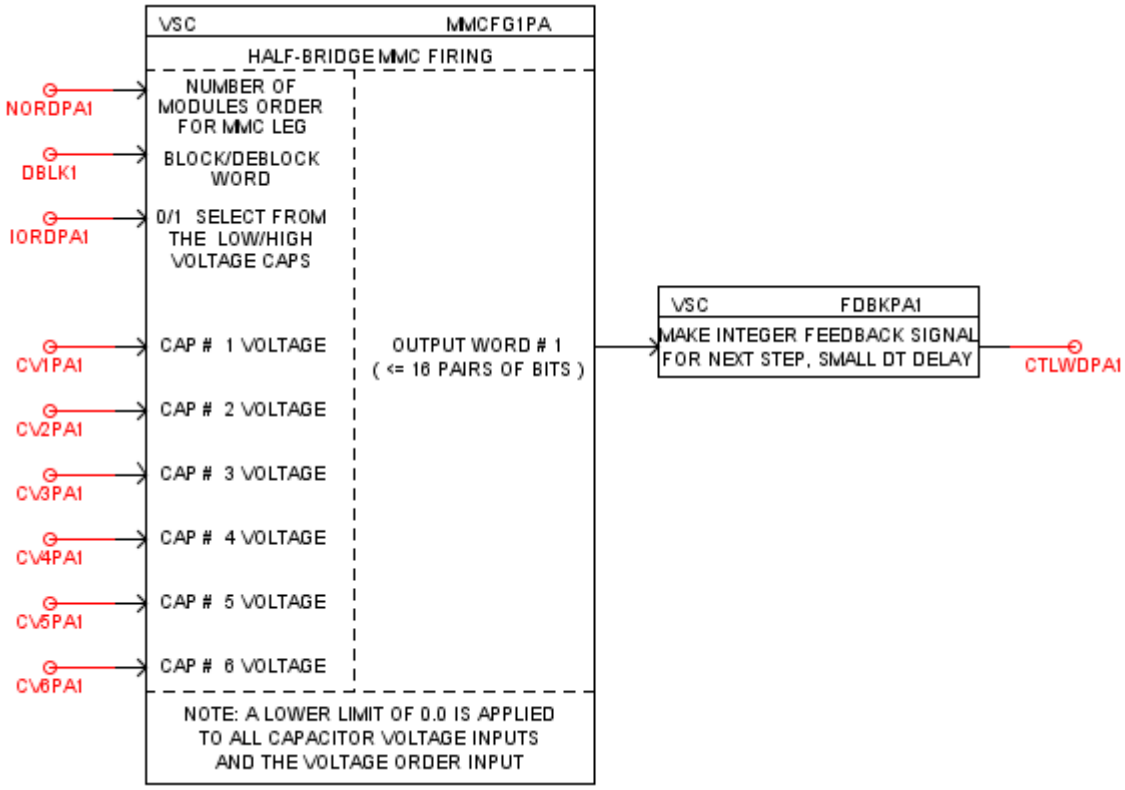


Figure 2-8 Capacitor balancing control in the RTDS

In Figure 2-8, *NORDijk* is the number of ON SMs and is generated from the NLM. *DBLKk* determines the blocking/deblocking of the MMC. *IORDijk* represents the direction of the arm current, which determines the charging/discharging of the SM capacitors. *CVmijk* (m = 1,…,6) are the monitored capacitor voltages. The output of the capacitor balancing controller, *CTLWDijk* is a 12-bit control word, which is the gating signal and contains information of the ON/OFF of each SM.

Under normal operating conditions, the SMs of the MMC are either charged/discharged with Mode 1 or bypassed with Mode 2. However, under transient conditions such as when the

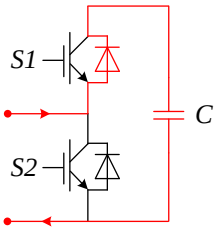
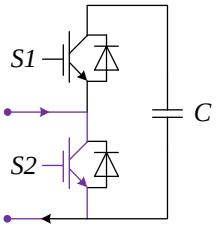
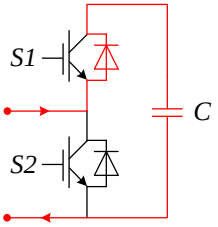
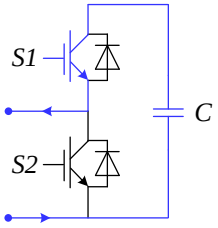
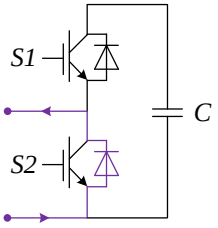
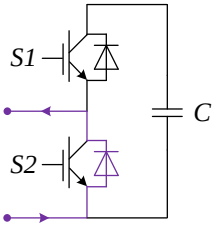
system is at the initial start-up stage or following a serious fault, the SMs are with another switching mode to protect the IGBTs:

- Mode 3: Both S1 and S2 are switched-off. Under this mode, all the IGBTs of the SMs within the MMC are blocked, i.e. the MMC is blocked. It has the following features:
  - The arm current is bidirectional;
  - The SM capacitor is either charged or bypassed depending on the direction of the arm current;
  - The MMC becomes to an uncontrollable diode bridge.

Mode 3 is also known as energisation mode.

Hence, all the operating modes of a SM are depicted in Table 2-1 [22].

Table 2-1 Operating Modes of a SM

Arm Current Capacitor Status	**Mode 1: Capacitor On**	**Mode 2: Capacitor Off**	**Mode 3: SM Blocked**
Charging Direction			
Capacitor Status	Charged	Bypassed	Charged
Discharging Direction			
Capacitor Status	Discharged	Bypassed	Bypassed

There are two main models available for MMC modelling in the RTDS, namely average model and detailed switching model. The MMC established for the test system in the RTDS uses the detailed switching model, namely VSC Chain Link Converter, which models the switching and charging/discharging dynamics of the SMs. An introduction of the average model and detailed switching model in the RTDS is provided in Appendix B.

2.3.3 Control Mode at Converter Level

At the converter level, the control mode of the MMC is similar to that of the traditional 2-level VSC in which the well-known *dq* decoupled control [68]-[69] is generally applied. The *dq* decoupled control consists of an inner current controller as shown in Figure 2-9 and an outer controller as shown in Figure 2-10.

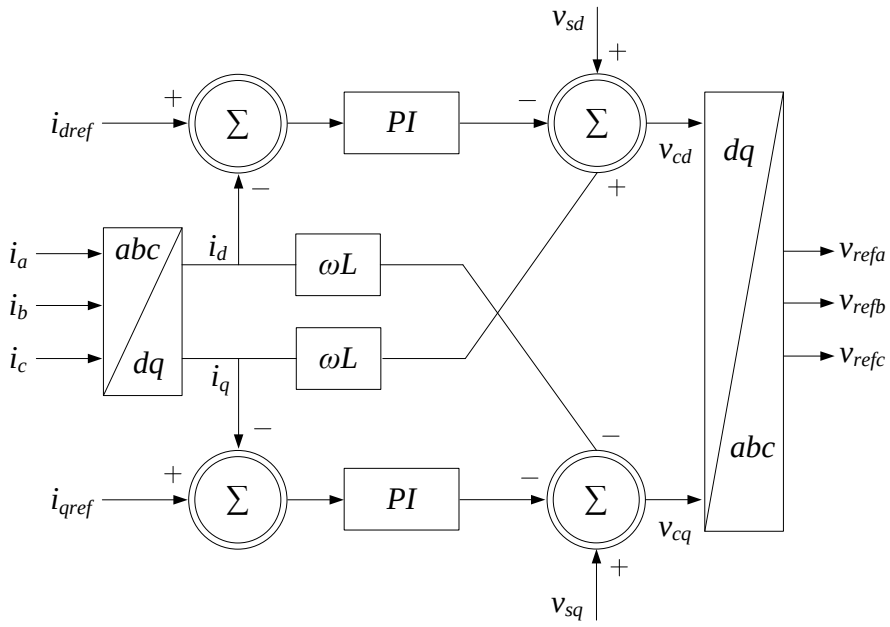


Figure 2-9 Inner current controller of the *dq* decoupled control

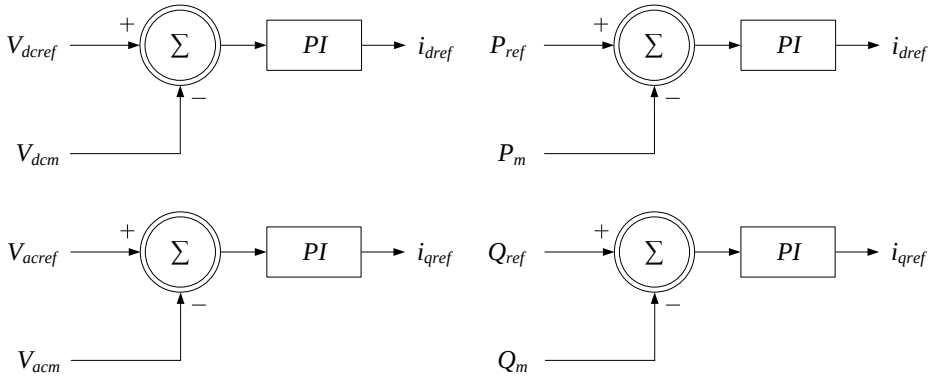


Figure 2-10 Outer controller of the *dq* decoupled control

In Figure 2-9, i_a, i_b, i_c are the three-phase AC line currents; i_d and i_q are currents on *d*- and *q*-axis after Park Transform [68]-[69]; v_{sd} and v_{sq} are the system voltage on the *d*- and *q*-axis; v_{cd} and v_{cq} are MMC AC-side voltage on the *d*- and *q*-axis; i_{dref} and i_{qref} are line current references on the *d*- and *q*-axis; v_{refa}, v_{refb}, v_{refc} are the voltage references at the MMC AC-side after inverse Park Transform. In Figure 2-10, V_{dcref} and V_{dcm} are the DC voltage reference and measurement; P_{ref} and P_m are the active power reference and measurement; V_{acref} and V_{acm} are the AC voltage reference and measurement; Q_{ref} and Q_m are the reactive power reference and measurement.

The following relationship can be derived from the inner current controller in Figure 2-9:

$$v_{cd} = v_{sd} - v_d^{'} + \omega L i_q \tag{2.3}$$

$$v_{cq} = v_{sq} - v_q^{'} - \omega L i_d \tag{2.4}$$

where

$$v_d^{'} = K_{p1}(i_{dref} - i_d) + K_{i1}\int (i_{dref} - i_d)dt \tag{2.5}$$

$$v_q^{'} = K_{p2}(i_{qref} - i_q) + K_{i2}\int (i_{qref} - i_q)dt \tag{2.6}$$

K_{p1} and K_{i1} are the proportional and integral coefficients of the inner current controller on the *d*-axis, while K_{p2} and K_{i2} are the proportional and integral coefficients of the inner current controller on the *q*-axis.

For the outer current controller in Figure 2-10, the following relationship can be derived:

For the *d*-axis, we have

$$i_{dref} = K_{p1}(V_{dcref} - V_{dcm}) + K_{i1}\int (V_{dcref} - V_{dcm})dt \tag{2.7}$$

$$i_{dref} = K_{p1}(P_{ref} - P_m) + K_{i1}\int (P_{ref} - P_m)dt \tag{2.8}$$

For the *q*-axis, we have

$$i_{qref} = K_{p2}(V_{acref} - V_{acm}) + K_{i2}\int (V_{acref} - V_{acm})dt \tag{2.9}$$

$$i_{qref} = K_{p2}(Q_{ref} - Q_m) + K_{i2}\int (Q_{ref} - Q_m)dt \tag{2.10}$$

Therefore, the *d*-axis can either regulate the DC voltage or the active power, while the *q*-axis can either control the AC voltage or the reactive power.

Apart from the *dq* decoupled control, another control mode, voltage-frequency (V_{ac}-*f*) control [49] as shown in Figure 2-11, is also generally applied by the VSC-type converters.

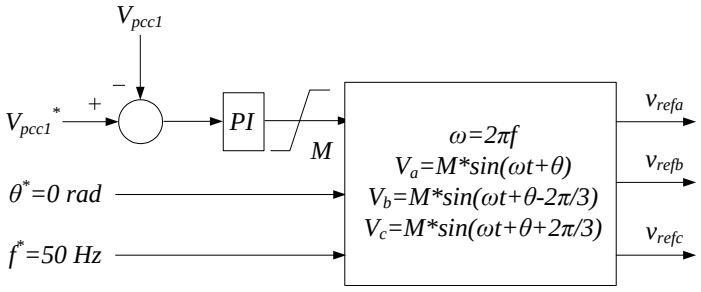


Figure 2-11 V_{ac}-f control

In Figure 2-11, V_{pcc1}^* and V_{pcc1} are the RMS AC voltage reference and measurement at the PCC. M is the modulation index and can be derived as:

$$M = K_{p3}(V_{pcc1}^* - V_{pcc1}) + K_{i3}\int (V_{pcc1}^* - V_{pcc1})dt \tag{2.11}$$

The control aim is to regulate the AC voltage magnitude and frequency at the PCC, which is mainly used for the connection of the network with power uncertainties, such as the load terminal or renewable energy sources.

For the offshore integrated 4-terminal MMC HVDC test system, the control mode of the converter at each terminal is: MMC-1 applies V_{ac}-f control; the other three terminals with active AC networks all use dq decoupled control where MMC-2 applies V_{dc}-Q control, both MMC-3 and MMC-4 apply P-Q control. Table 2-2 shows the control mode of each MMC.

Table 2-2 Control Modes of the MMCs

Onshore MMC	**Control Strategy**	
MMC-1	V_{ac}-f	
Offshore MMC	***d*-axis**	***q*-axis**
MMC-2	V_{dc}	Q
MMC-3	P	Q

MMC-4	*P*	*Q*

2.3.4 Reference Settings at System Level

At the system level, the control settings under steady-state and transient conditions are mainly based on the system parameter design and operating requirement. Under steady-state conditions, the control references are set to make the system work stably within the operating range. The reference settings of the MMCs are shown in Table 2-3.

Table 2-3 Control Reference Settings of the MMCs

MMC-*n*	**Control Reference Setting**
MMC-1	V_{ac} = 1 p.u., f = 50 Hz
MMC-2	V_{dc} = ±50 kV, Q = 0 MVar
MMC-3	P = 50 MW, Q = 0 MVar
MMC-4	P = -90 MW, Q = 0 MVar

Under transient conditions, the control references are dynamically adjusted according to the system performance. For example, during the system start-up, the DC voltage and active power reference are dynamically adjusted to smooth the performance; under fault conditions, control and protection signals need to have speedy response to provide effective protection; after the isolation of the faulted section line, the recovery control is activated to co-ordinately resume each terminal. The detailed dynamic adjustment on the system control, protection and recovery will be described in the later chapters.

2.4 Offshore Wind Farm

There are two types of generators that are most commonly used [120], doubly-fed induction generator (DFIG) and permanent magnet synchronous generator (PMSG), for wind power applications. For the DFIG, only 25%-30% of the rated power is generated in the rotor and then fed into the back-to-back converter. Hence, the cost of the converter in the DFIG is much lower than the full rated converter in a PMSG [120]–[123]. In addition, the footprint of a DFIG is generally smaller than that of a PMSG with a same rating. There have been an increasing number of wind power applications including OWF applications of using DFIGs [124].

The OWF used in the test system is doubly-fed induction generator (DFIG) type and consists of numerous DFIGs. In the test system, the OWF consists of 60 DFIGs where the output power of each DFIG is 1.4 MW. The modelling of the OWF is through the modelling of the characteristics of one DFIG and scaling it up to many DFIGs to form an OWF. The following sub-sections will describe the structure and basic control strategy of the DFIG.

2.4.1 DFIG Structure

Figure 2-12 presents the structure of a DFIG [125]–[126]. The wind turbine is connected with the induction generator (IG) via a gear box which matches the rotational speed of the wind turbine with that of the IG. This is because the rotational speed of the wind turbine is generally much lower than that of the IG. The stator side of the IG is directly connected to the grid via a three-phase three-winding transformer. However, the rotor side of the IG is firstly connected with a back-to-back converter consisting of two VSCs and a DC capacitor and then connected to the grid through the transformer. The VSC close to the rotor side of the IG is called *Rotor VSC*, while the other VSC close to the grid side is called *Grid VSC*.

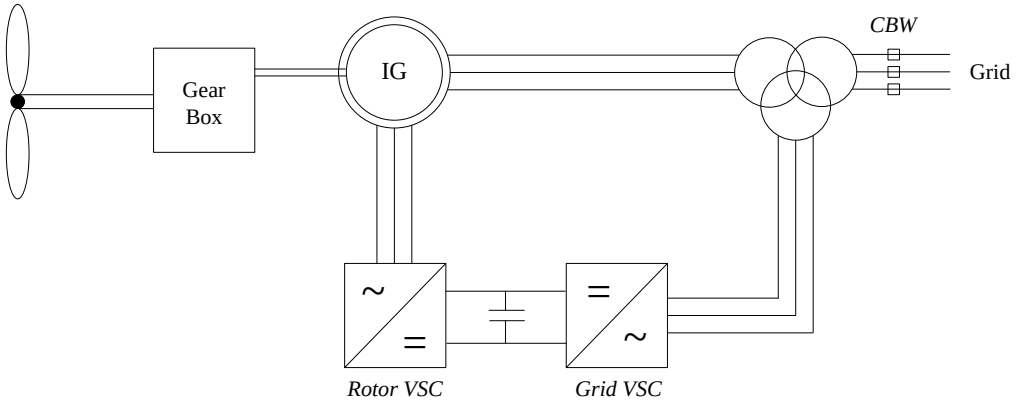


Figure 2-12 Structure of one DFIG [125]-[126]

2.4.2 Basic Control Strategy of a DFIG

The control of a DFIG on the stabilisation of its terminal voltage and output power is mainly through the effective control on the back-to-back converter. The control strategy applied on the back-to-back converter of the DFIG is based on [125]. Both VSCs apply *dq* decoupled control to achieve independent control on the active and reactive power. The *d*-axis of the *Grid VSC* controls the DC voltage of the capacitor and the *q*-axis controls the reactive power. The *d*-axis of the *Rotor VSC* regulates the electrical torque to track the optimal power out of the wind turbine and the *q*-axis regulates the rotor excitation current to control the reactive power. The basic control strategy of the DFIG is shown in Table 2-4.

Table 2-4 Control Strategy of the DFIG

DFIG	**Control Strategy**	
Back-to-back converter	***d*-axis**	***q*-axis**
Grid VSC	V_{dc}	*Q*
Rotor VSC	*P*	*Q*

For the operation of DFIG-type wind farm, particularly OWF, one key requirement is the low

voltage ride-through (LVRT) capability. That is, the DFIG should be able to continue operation through periods when the grid has a lower voltage but is larger than the minimum specified condition, which is either caused by a disturbance or a fault on the AC network, to support the grid voltage [127]–[130]. Otherwise, if one DFIG is disconnected with the AC network without providing support to the grid voltage, it will result in a further decrease in the grid voltage and cause other generators to disconnect consecutively. It may finally lead to chain reaction and cascading failure. Figure 2-13 presents a typical LVRT requirement which is defined by the grid code [130].

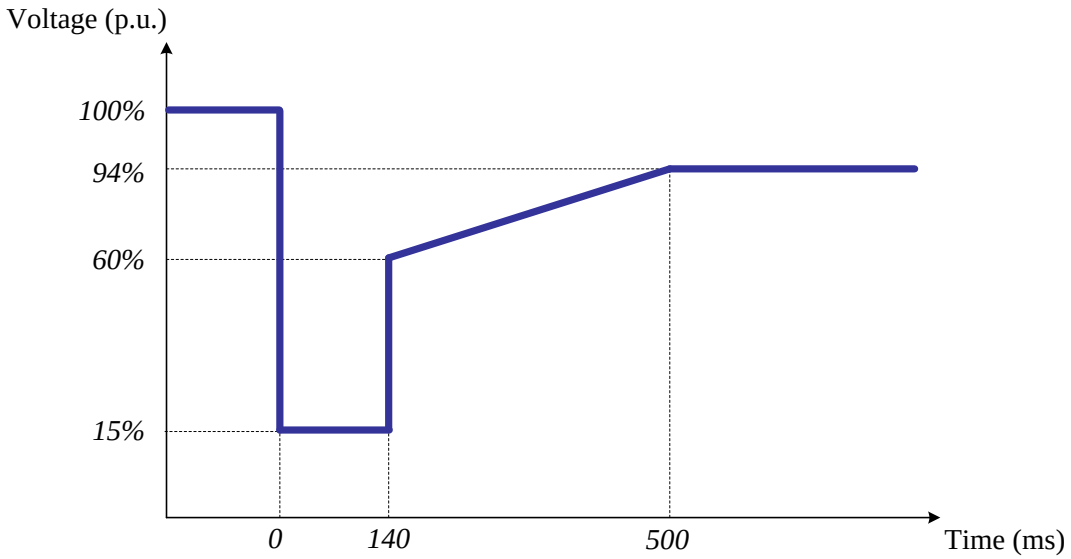


Figure 2-13 LVRT requirement [130]

The vertical points of the blue line represent the grid voltage level, while the herizantal points of the line represent the associated time. According to [130], the converter must remain connected to the system without tripping for a fault up to 140 ms as shown in Figure 2-13 [131]. If the voltage level is below the blue line, disconnection of the converter is permitted. Otherwise, the converter must stay connected during the associated period to support the grid voltage during the fault. The LVRT is not the focus of this thesis and is only briefly

introduced.

2.5 Summary

In this chapter, the configuration of the offshore integrated MMC MTDC test system has been presented. Two main components of the test system, the MMC and OWF, have been described. For the MMC, its structure has been presented and introduced. The operating mode at the valve level, control mode at the converter level and reference settings at the system level have been described. For the DFIG-based OWF, the DFIG structure and its basic control strategy have been presented. This chapter provides fundamental descriptions and information of the test system for the following chapters.

CHAPTER 3 STEADY-STATE, POWER BALANCING AND POWER FLOW REVERSAL OF THE MMC MTDC SYSTEM WITH AN OWF

The objectives of this chapter are 1) to calculate the system operating condition under the nominal steady-state; 2) to propose an assumption on the maximum allowable voltage and current during transient conditions; 3) to present the system power balancing and power flow reversal performance.

3.1 Introduction

In this chapter, the system performance under the nominal steady-state condition and transient conditions from one steady-state to another steady-state, including 1) change of wind speed; 2) wind intermittency; 3) power ramping at one terminal; 4) power flow reversal, is investigated. Under the nominal steady-state with the control modes and control reference settings described in Chapter 2, the system operating condition of the voltages, currents and power at the AC and DC sides is calculated. According to the system operating status, an assumption on the maximum allowable values of the voltages and currents during transient conditions is proposed. This assumption can be applied for the validation of the control performance during transients, including that of the power balancing and power flow reversal, start-up control, control and protection under fault conditions.

3.2 Steady-State Condition

3.2.1 Nominal Steady-State Calculation

The nominal steady-state condition defined in this thesis is when the system is working with the control modes and references as described in Chapter 2. The system status under this condition, which is the values of the voltages and currents at both sides of the MMCs, can be calculated using the system parameters shown in Appendix A and control reference settings shown in Table 2-3. During the calculation, the power losses on the MMCs and the DC cable are not considered and the DC voltage at each terminal is assumed to be maintained at ±50 kV. The calculation results of the system status under nominal steady-state condition are presented in Table 3-1.

Table 3-1 System Status under the Nominal Steady-State Condition

System Status	T1	T2	T3	T4	Comments
AC voltage at the PCC	138 kV	138 kV	138 kV	138 kV	L-N, RMS
AC current at the PCC	0.20 kA	-0.11 kA	0.12 kA	-0.22 kA	
Active power at the PCC	84 MW	-44 MW	50 MW	-90 MW	
Reactive power at the PCC	-10 MVar	0 MVar	0 MVar	0 MVar	
MMC AC-side voltage	30 kV	30 kV	30 kV	30 kV	L-N, RMS
MMC AC-side current	0.93 kA	-0.49 kA	0.56 kA	-1 kA	
DC terminal voltage	±50 kV	±50 kV	±50 kV	±50 kV	
DC terminal current	0.84 kA	-0.44 kA	0.5 kA	-0.9 kA	

3.2.2 Transient Assumption

The operation of power systems, including the modern power systems with FACTS and HVDC, should meet the requirement of the grid code [130]. However, due to the fact that the MTDC based on VSC technology are a very recent research subject, there has been no comprehensive standard or benchmark system for the operation of VSC MTDC systems [24],

[132]. An assumption is made in this section for the operation of the investigated MTDC under transient conditions. Since the nominal power rating is 150 MVA and the nominal DC voltage is ±50 kV, the DC current transferred at the full capacity is 1.5 kA. During transient conditions, the maximum allowable DC currents are assumed to be 20% over that at the full capacity, which is also the control objective to limit the currents under 1.8 kA. Similarly, as for the DC voltages, AC voltages and AC currents, they are all expected to be controlled within 20% over the full rated value during system transients. These assumptions are mainly used for the system under severe fault conditions, such as AC and DC faults. Apart from the fault conditions, it is expected to limit the currents and voltages within 5% of the full capacity.

3.3 Transient Conditions between Two Steady-States

This chapter investigates 4 transient conditions where each condition is a transition from one steady-state to another steady-state. They are: 1) change of wind speed; 2) wind intermittency; 3) power ramping at one terminal; 4) power flow reversal. The following sub-sections will describe each condition and demonstrate simulation case studies on the RTDS.

3.3.1 Change of Wind Speed

The nominal wind speed for the OWF is 12 m/s and its output power under this speed is 84 MW. When the wind speed rapidly drops to 10 m/s, the output power will decrease consequently and the system will achieve a new steady-state. The measuring points of the MTDC in the simulations in this chapter and the later chapters are illustrated in Figure 3-1. P_n and Q_n (n = 1,…,4) denote the active power and reactive power measured at the PCC; V_{cn} and I_{cn} (n = 1,…,4) denote the MMC AC-side voltage and current measured in RMS value; V_{dcn} and I_{dcn} (n = 1,…,4) denote the DC voltage and current measured at each terminal. The

reference directions of the currents and power are illustrated in Figure 3-1.

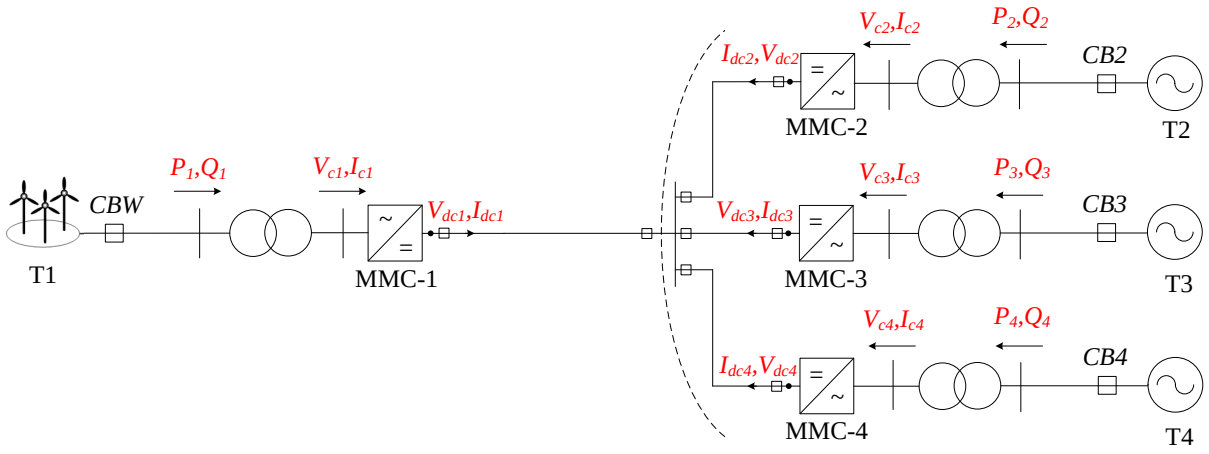
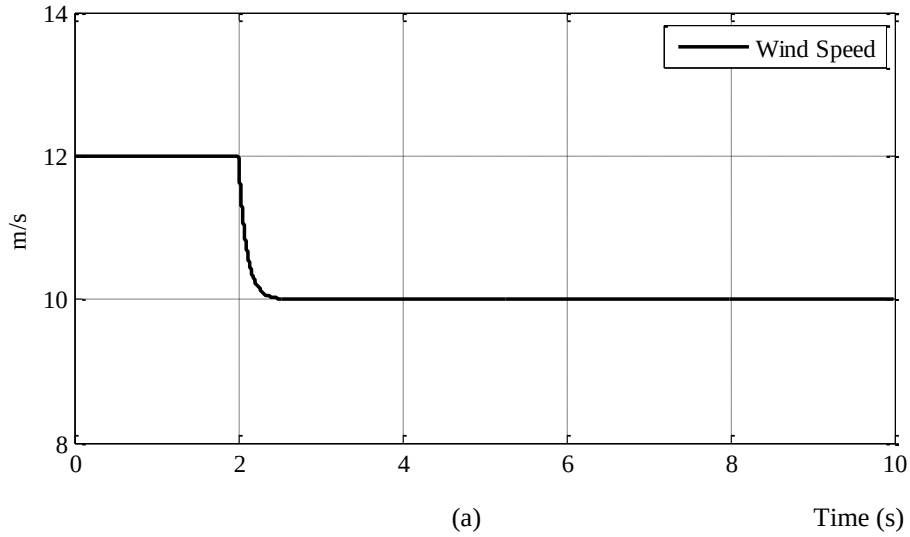
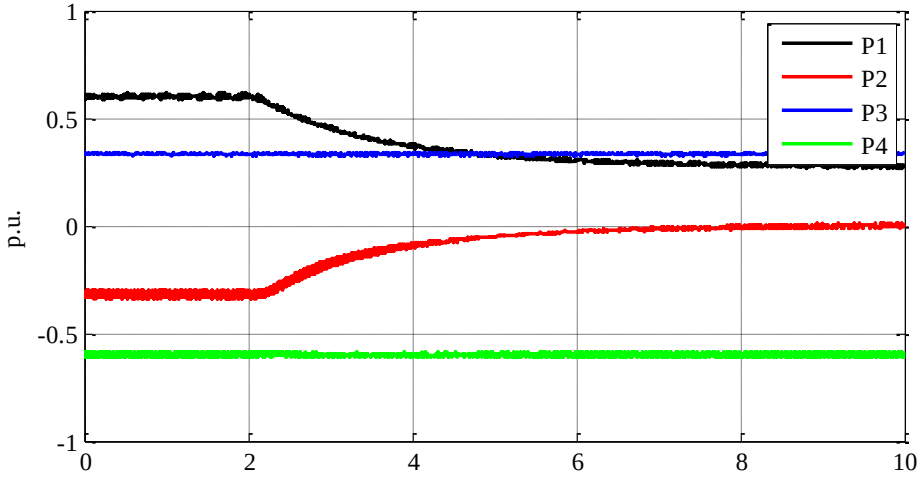


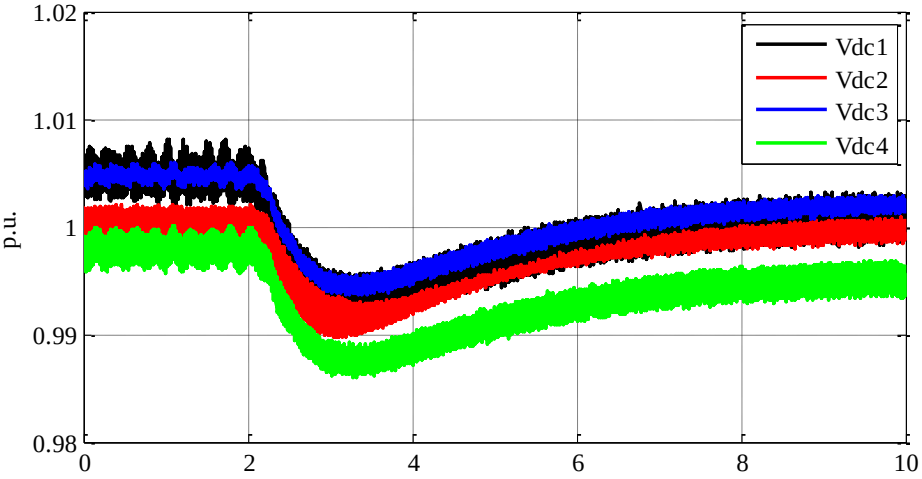
Figure 3-1 Measuring points of the MTDC

The system performance using the RTDS simulation is demonstrated in Figure 3-2: (a) wind speed; (b) active power; (c) DC voltages; (d) DC currents; (e) MMC AC-side voltages in RMS value; (f) MMC AC-side currents in RMS value.

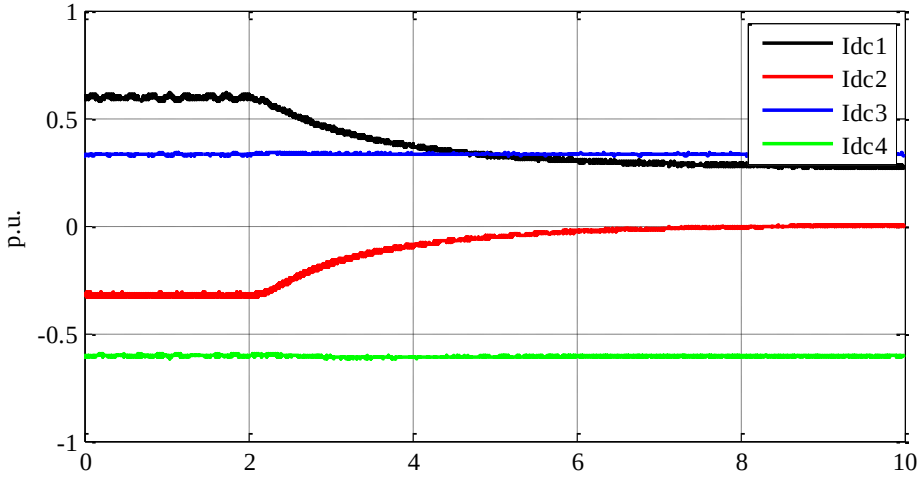




(b) Time (s)



(c) Time (s)



(d) Time (s)

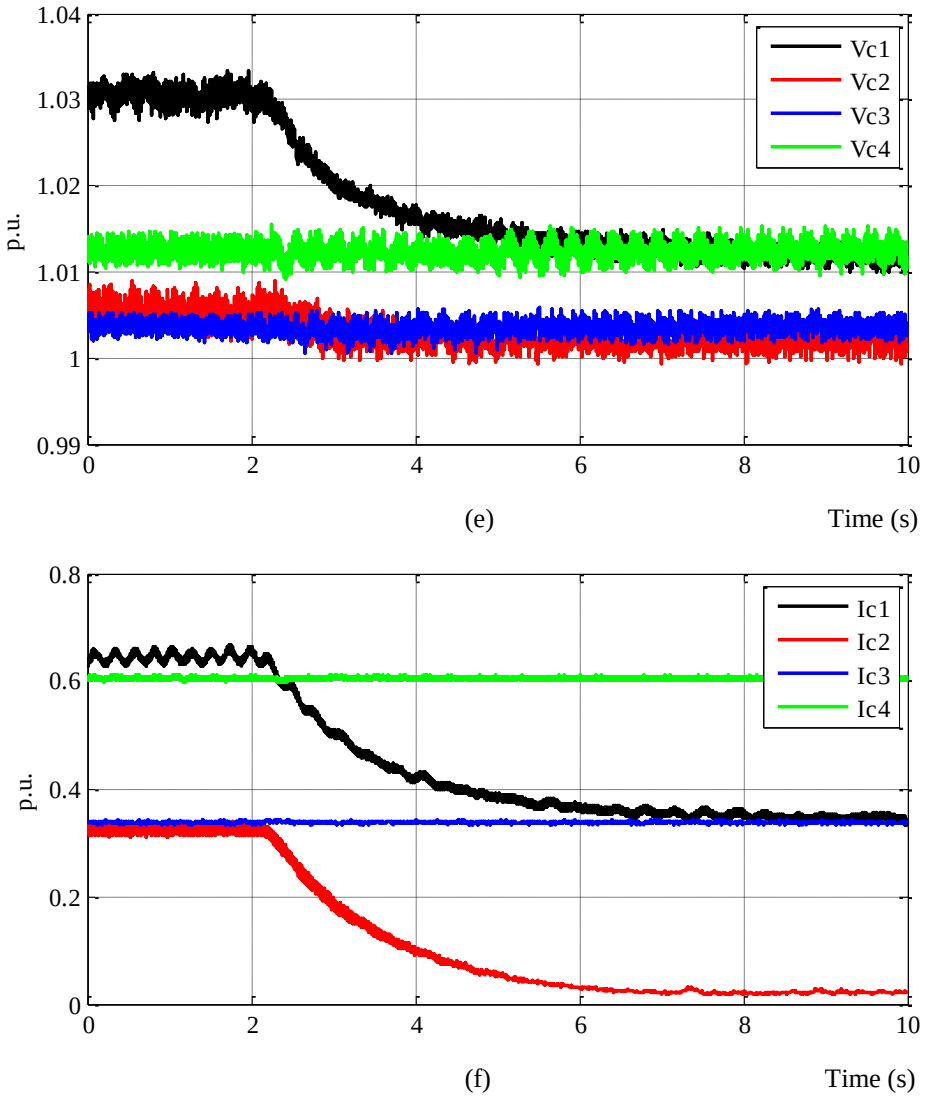


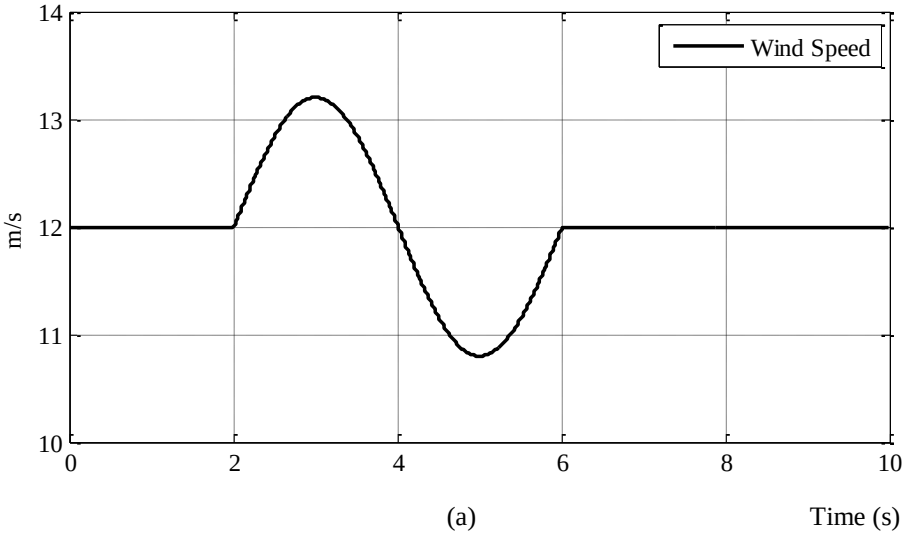
Figure 3-2 System performance under changes of wind speed

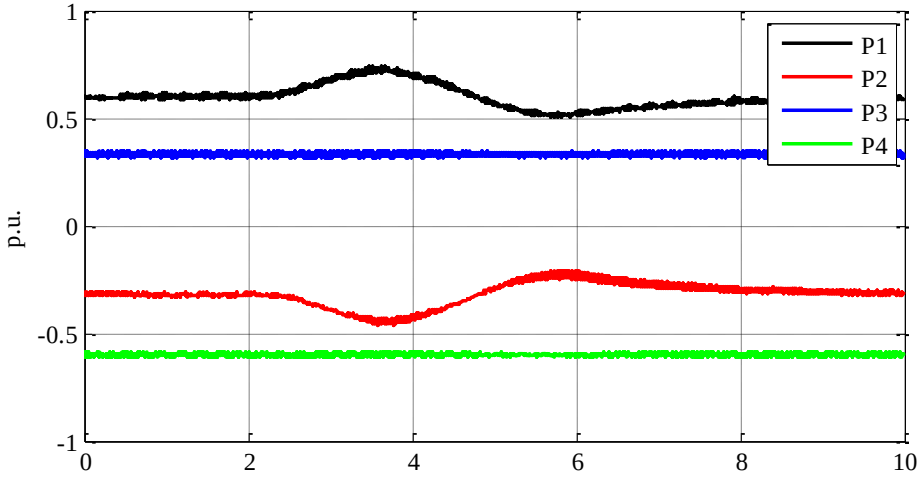
The wind speed drops from 12 m/s to 10 m/s at 2 s as shown in Figure 3-2(a). Figure 3-2(b) shows that the active power at T1 decreases from 0.56 p.u. to 0.28 p.u.. The reduced active power is compensated by the master terminal T2 which is operated as a DC slack bus. T3 and T4 maintain the original power transfer. Figure 3-2(c) demonstrates that the DC voltages are soon stabilised after a small voltage dip. The DC currents and the MMC AC-side currents at T1 and T2 reach a new steady-state as shown in Figure 3-2(d) and Figure 3-2(f), respectively. In Figure 3-2(c), a sinusoidal pattern of the DC voltage at T1 can be observed from 0 s to 2 s.

This is because T1 is connected with the OWF and the wind turbine is modelled using detailed mechanical turbine model which simulates the dynamics of the output power of the OWF. Similar phenomenon can be observed in Figure 3-2(f). An introduction of the mechanical model for the wind turbine is provided in Appendix C.

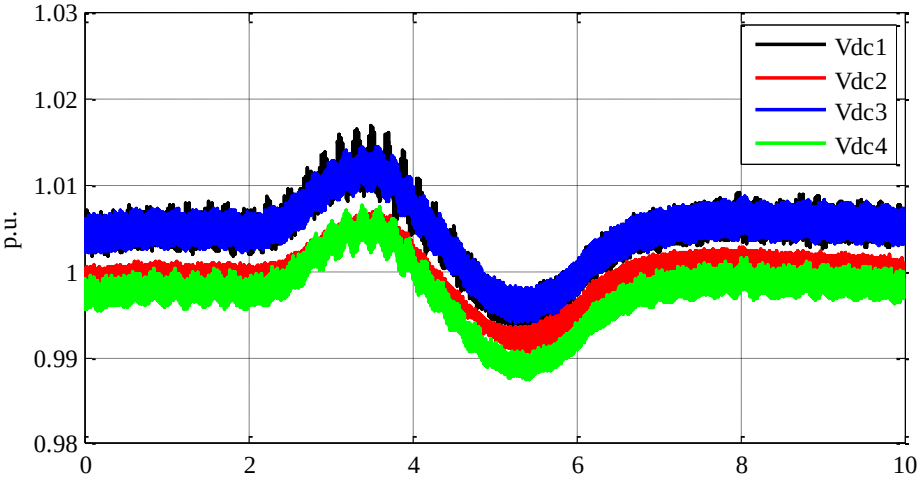
3.3.2 Wind Intermittency

Due to the inherent intermittent characteristics of wind power, a transient condition, where the 12 m/s wind speed experiences fluctuations with 1.2 m /s amplitude and 0.25 Hz frequency for 4 s, is simulated on the RTDS. The system performance is shown in Figure 3-3: (a) wind speed; (b) active power; (c) DC voltages; (d) DC currents; (e) MMC AC-side voltages in RMS value; (f) MMC AC-side currents in RMS value.

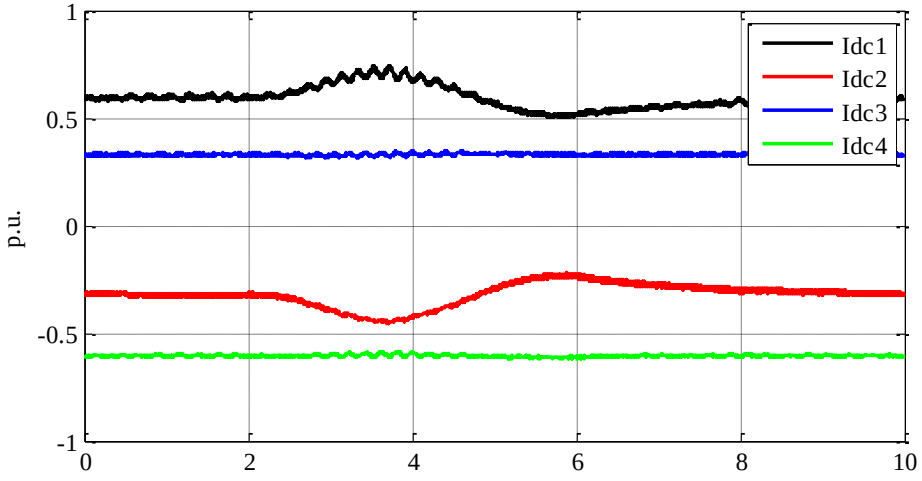




(b) Time (s)



(c) Time (s)



(d) Time (s)

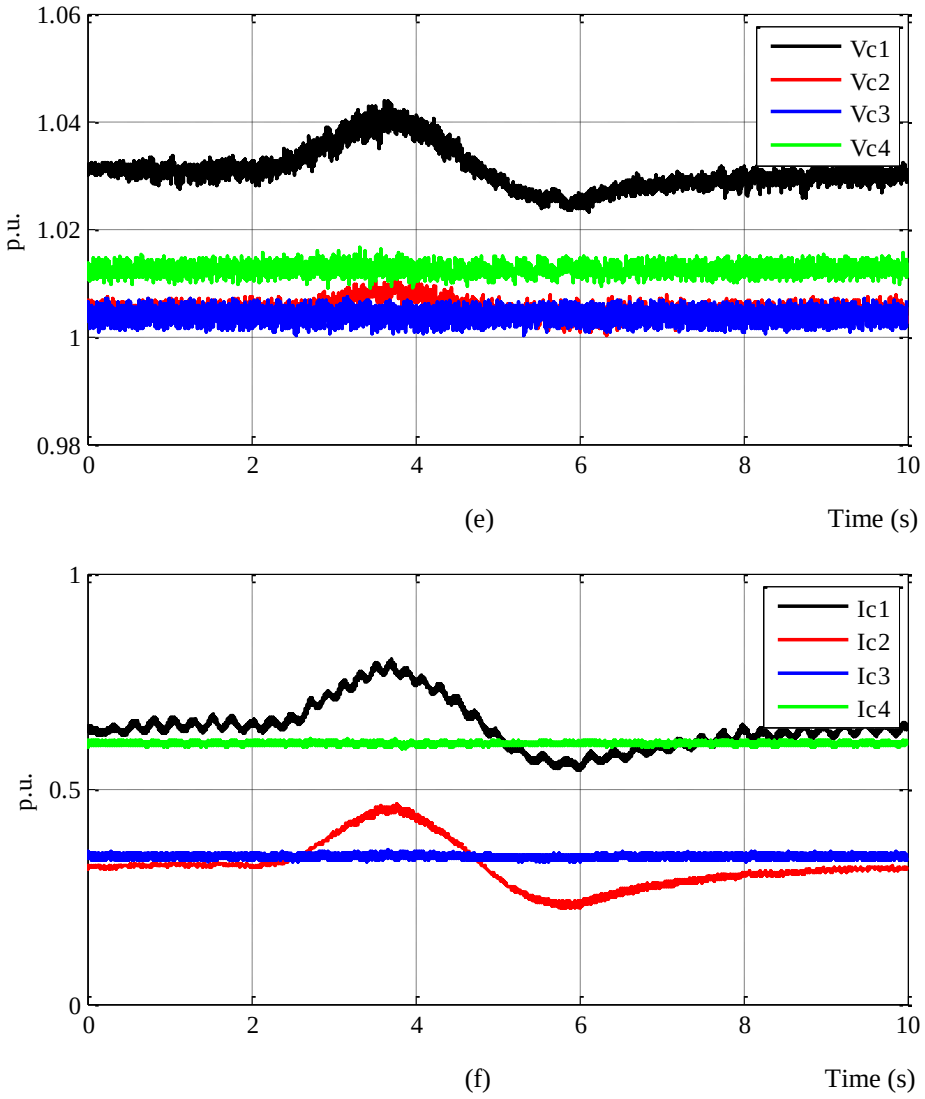
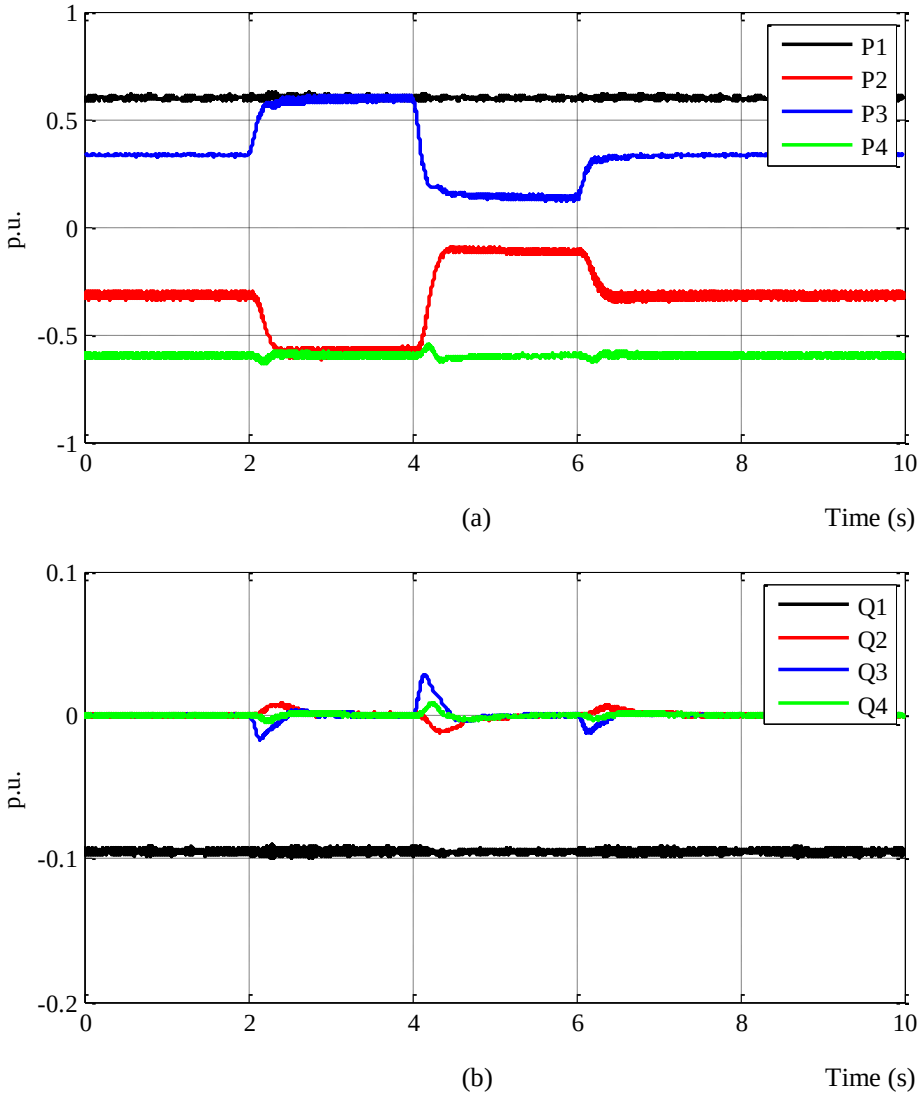


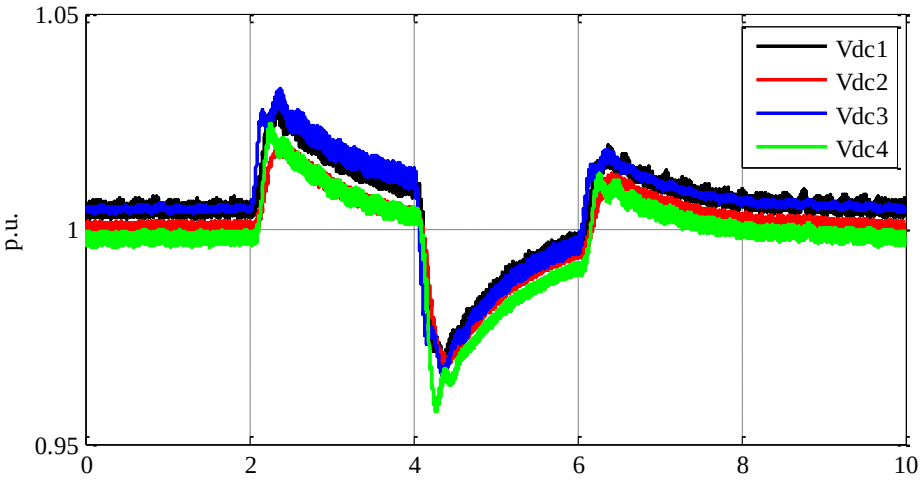
Figure 3-3 System performance under intermittent wind condition

Figure 3-3(a) shows the fluctuations of the wind speed with 1.2 m/s amplitude between 2 s and 6 s. Figure 3-3(b) shows the oscillations of the active power at T1 and T2. Small voltage oscillations can be observed in Figure 3-3(c) during the wind intermittency. The performance of the DC and AC currents follows that of the active power as shown in Figure 3-3(d) and (f). Figure 3-3(e) demonstrates small voltage oscillations generated at the AC side of MMC-1.

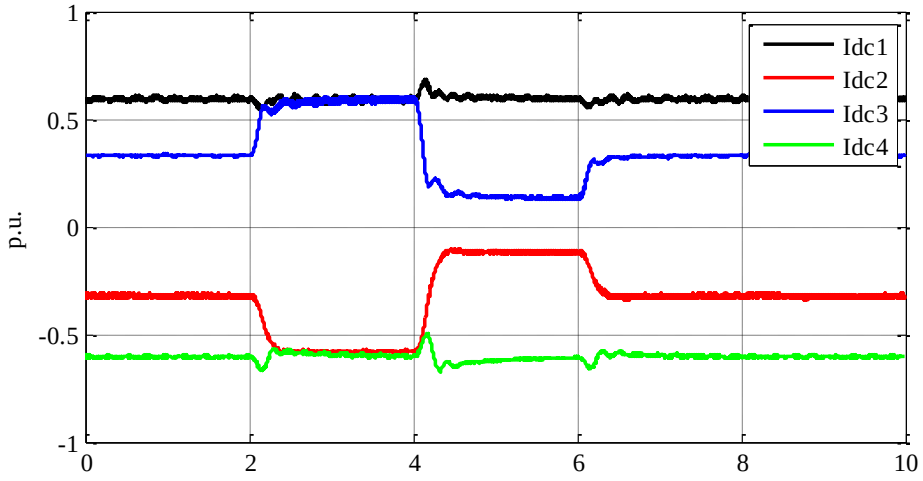
3.3.3 Power Ramping

When the power dispatcher, T3 or T4, changes the active power reference, the active power of the MTDC will be balanced by the master terminal T2. A transient condition, where the active power of T3 ramps up from 50 MW to 90 MW and then ramps down to 20 MW and finally resumes to 50 MW, is simulated on the RTDS. The system performance is demonstrated in Figure 3-4: (a) active power; (b) reactive power; (c) DC voltages; (d) DC currents; (e) MMC AC-side voltages in RMS value; (f) MMC AC-side currents in RMS value.

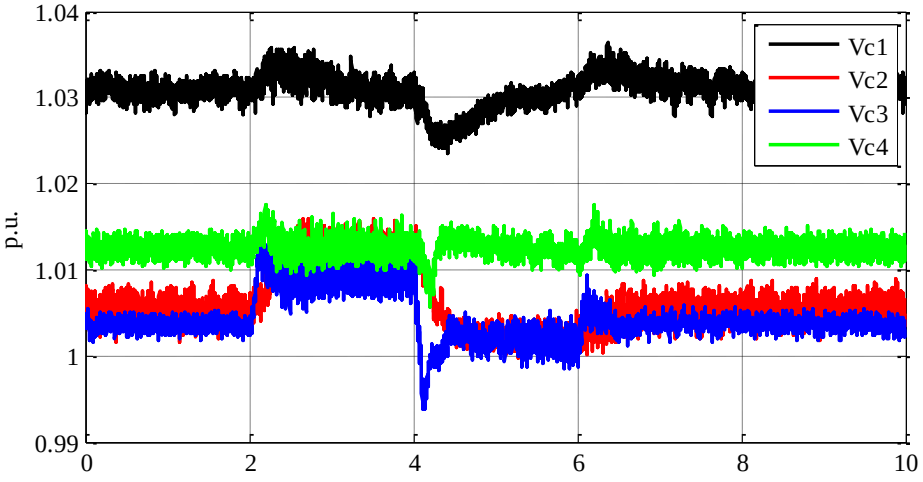




(c) Time (s)



(d) Time (s)



(e) Time (s)

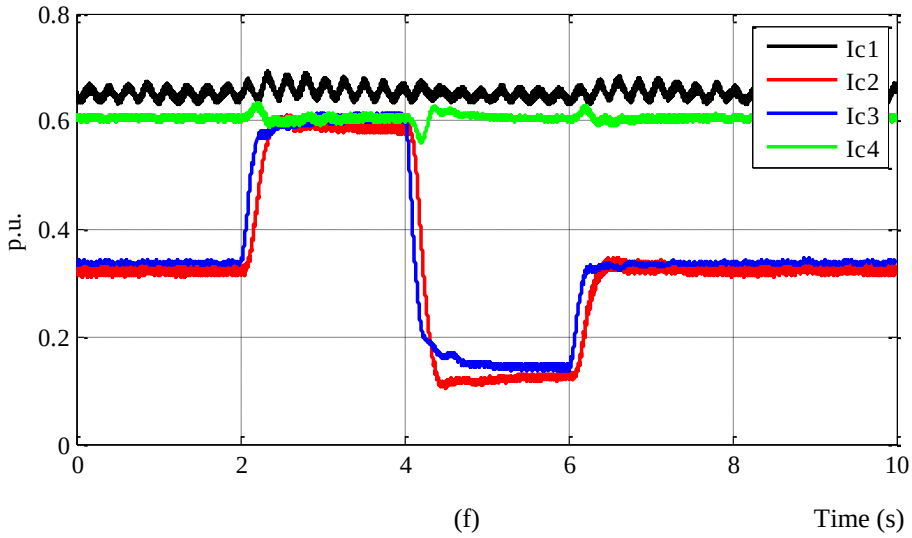


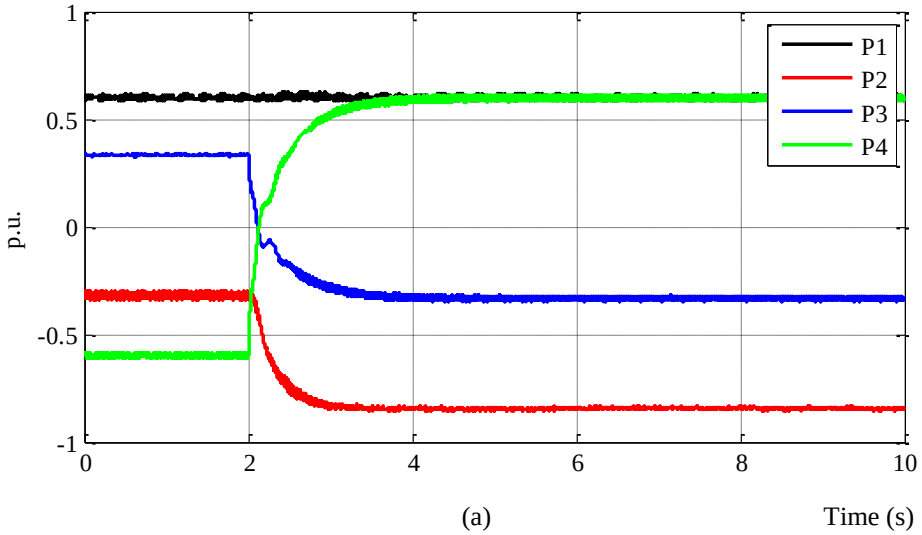
Figure 3-4 System performance under power ramping

Figure 3-4(a) demonstrates the changes of the active power at T3 at 2 s, 4 s and 6 s, which are compensated by those of T2. Figure 3-4(b) shows the reactive power is not influenced during the period due to the *dq* decoupled control of active and reactive power. The DC voltages and MMC AC-side voltages are both well stabilised as shown in Figure 3-4(c) and (e). The changes of the DC currents and MMC AC-side currents have the same pattern to those of the active power as demonstrated in Figure 3-4(d) and (f), respectively.

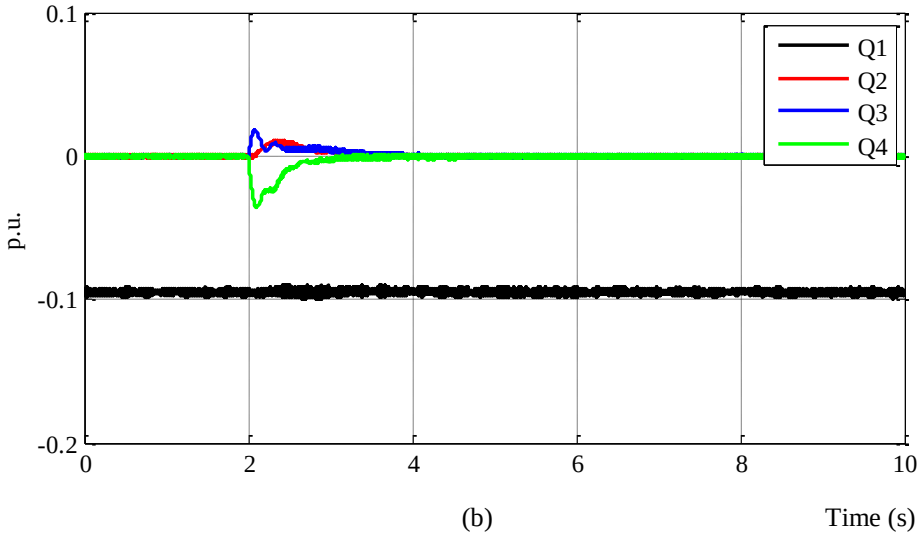
3.3.4 Power Flow Reversal

The capability of power flow reversal is important for MTDC systems. It enables the system to flexibly change the direction of the active power according to the system operating condition. Since the OWF terminal is always feeding power into the DC grid under normal operating condition, a power flow reversal of the other three terminals, where the reference power of T3 and T4 is reversed and T2 compensates the changes of power, is simulated on the RTDS. The system performance is demonstrated in Figure 3-5: (a) active power; (b) reactive power; (c) DC voltages; (d) DC currents; (e) MMC AC-side voltages in RMS value; (f) MMC

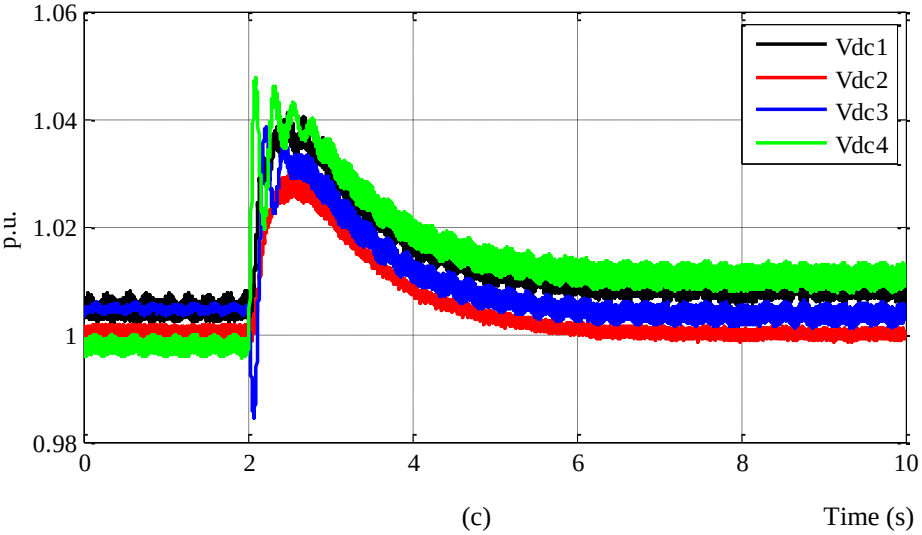
AC-side currents in RMS value.



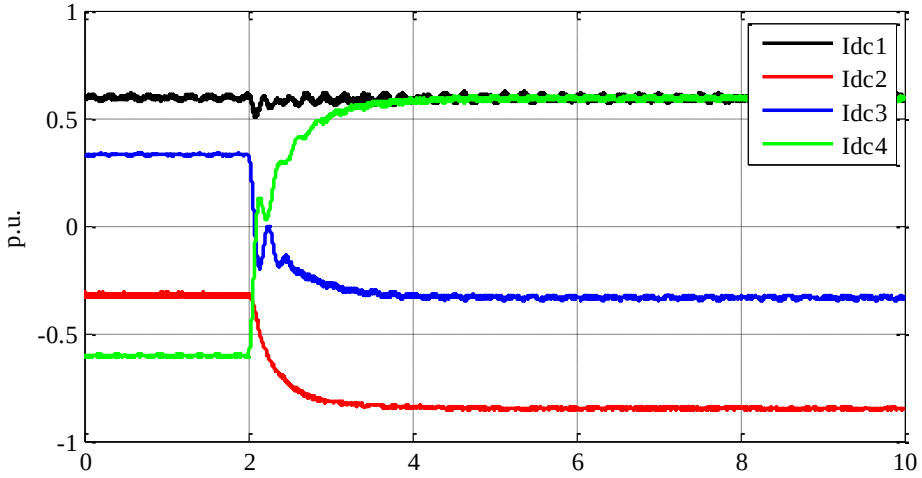
(a)

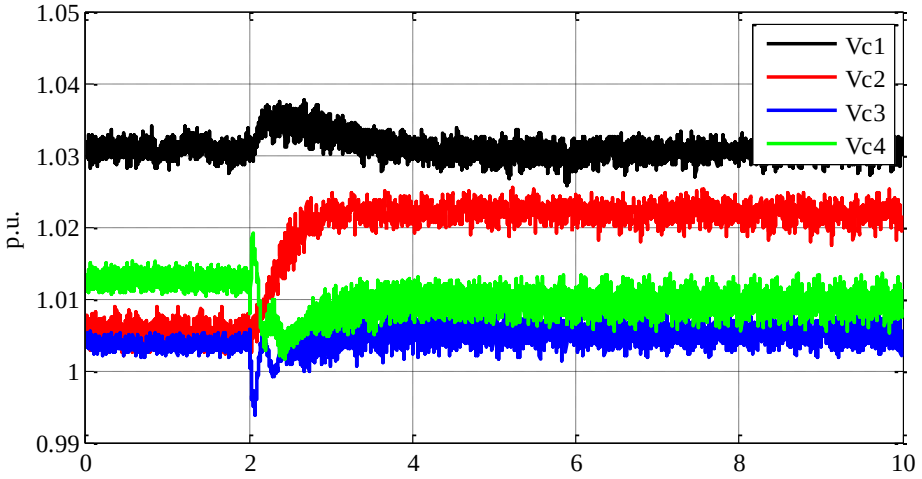


(b)



(c)





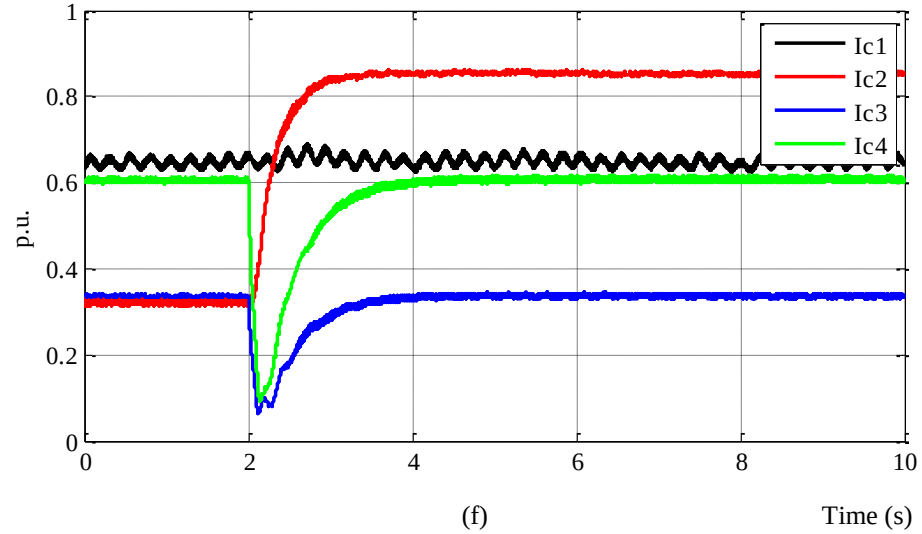


Figure 3-5 System performance under power flow reversal

Figure 3-5(a) demonstrates the power flow reversal at T3 and T4, while T2 balances the power change and T1 maintains its power transfer. The DC voltages have a small rise at the beginning of the power flow reversal and soon resumes to steady-state condition as demonstrated in Figure 3-5(c). The DC voltages at T3 and T4 have oscillations for around 0.7 s, while the DC voltages at T1 and T2 do not oscillate. This phenomenon could be caused due to the fact that the control strategies of MMC-3 and MMC-4 are the same, but are different with those of MMC-1 and MMC-2. Figure 3-5(d) and (f) shows that the currents change smoothly at the MMC DC- and AC-side, respectively.

3.4 Summary

In this chapter, the system status under the nominal steady-state has been calculated, providing the nominal values of the voltages, currents, active and reactive power of the system. Under transient conditions, the control objectives on the electrical quantities have been given. This has provided the foreshadowing and an assumption under transient conditions, for the investigation of the MTDC performance of the transition between two steady-states in this chapter and the start-up control, control and protection under fault conditions in the later chapters.

The MTDC performance under 1) change of wind speed; 2) wind intermittency; 3) power ramping; 4) power flow reversal, has been analysed with real-time simulations. This chapter has provided the basic characteristics and capability of the system, including adaption to wind uncertainty, capability of power balancing and power flow reversal, which has been demonstrated and justified.

CHAPTER 4 START-UP CONTROL OF THE MMC MTDC SYSTEM WITH AN OWF

The aim of this chapter is to analyse the system start-up characteristics and investigate the start-up control. The objective of the start-up control is to start the system in a stable and smooth manner with small voltage spikes and current surges.

4.1 Introduction

The test system has 1 offshore terminal connected with an OWF and 3 onshore terminals connected with AC utility grids. The system state before start-up is that all AC circuit breakers and the DC isolation switches are open and that the MMCs and the OWF are blocked as illustrated in Figure 4-1.

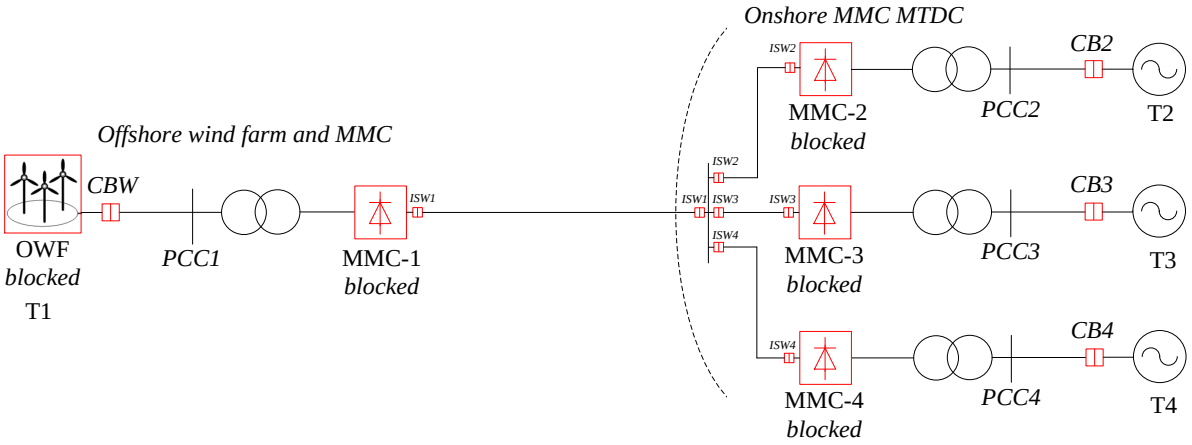


Figure 4-1 System state before start-up

At the initial stage, the OWF cannot provide any power nor can it support the AC voltage, so the offshore terminal is regarded as a passive network. The onshore terminals are connected with AC voltage sources and are regarded as active networks.

For the sake of simplicity, the DC isolation switches are assumed to be closed at the initial stage of the start-up control. For the start-up process after that, the characteristics of the terminals with active networks are significantly different to those of the terminal with a passive network. The onshore MMCs all apply *dq* decoupled control, while the offshore MMC applies V_{ac}-f control, as shown in Table 2-2. Because of these differences, in the following sections, we will separately investigate the start-up process and control of 1) the onshore terminals; 2) the offshore terminal. For the onshore MMCs, although they all apply *dq* decoupled control, the control modes are not exactly the same where one of them applies V_{dc}-Q control and the other two apply P-Q control as shown in Table 2-2. Moreover, the reference settings of them are different as shown in Table 2-3. Therefore, the start-up process and control are divided into *A.* before the deblocking of the MMC; *B.* after the deblocking of the MMC [133]. Combining the start-up control of the onshore terminals, T2, T3 and T4, a hierarchical start-up control for the active AC network connected MMCs is proposed. For the offshore terminal, a start-up scheme with reduced DC voltage control is proposed. According to the analysis of the whole start-up process, a combination of the start-up control of both the onshore and offshore terminals forms a comprehensive start-up control sequence for the whole system. The proposed sequence is verified through RTDS simulations.

4.2 Start-Up Process and Control of the Onshore Terminals with Active AC Networks

4.2.1 Before the Deblocking of the MMCs

For the active AC network connected terminal, the AC circuit breaker is closed prior to the deblocking of the MMC, so as to charge the AC network, the SM capacitors of the MMC and

the DC cable. Taking one terminal as an example, the current system state is illustrated in Figure 4-2.

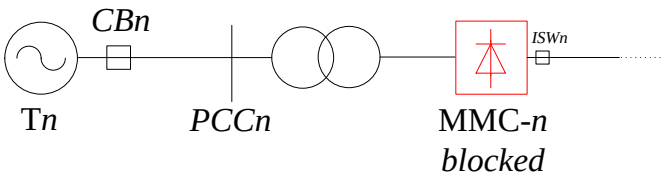


Figure 4-2 System state after closing the AC circuit breaker

At this stage, the operating mode of the MMC at the valve level is Mode 3 in Table 2-1 with all SMs blocked. Under this condition, the MMC is operated as an uncontrolled diode bridge, a detailed structure of which is depicted in Figure 4-3 [86], [133].

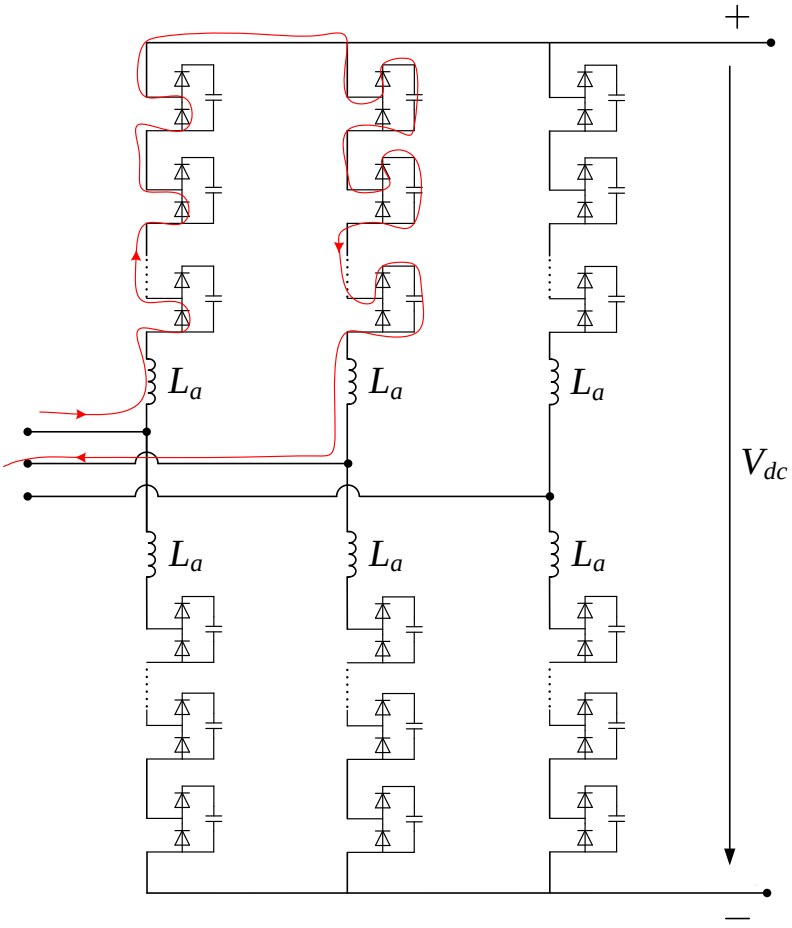


Figure 4-3 MMC with blocked state [86], [133]

One of the charging current flows is illustrated by the red solid line. By considering the losses of the diodes and circuit resistors, the current charging state of the MMC and its AC side can be simplified and illustrated as shown Figure 4-4(a), where $\hat{u}_l$ is the magnitude of the line voltage of the transformer secondary side; R_s is the line resistance between the transformer secondary side and the MMC AC side; L_a is the MMC arm inductance; R_d is the resistance of one diode; C is the capacitance of one SM; n is the number of SMs per arm. It can be further simplified to an RLC circuit as shown in Figure 4-4(b), where $R_{eq} = 2R_s + 2nR_d$, $L_{eq} = 2L_s + 2L_a$, $C_{eq} = C/n$, $U_0 = \hat{u}_l$. In Figure 4-4(b), u_R, u_L, u_C are the voltages of R_{eq}, L_{eq}, C_{eq}, respectively.

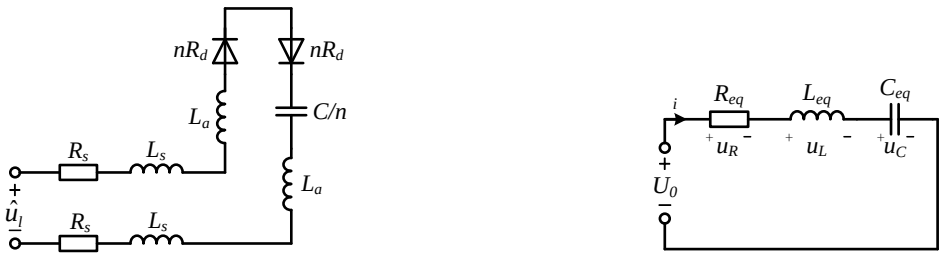


Figure 4-4 Equivalent RLC circuit before deblocking of the MMC: (a) equivalent circuit, (b) simplified circuit

This is a second-order RLC circuit. The initial state of the circuit when closing the AC circuit breaker can be expressed as

$$i_L(t_{0+}) = i_L(t_{0-}) = i(t_0) = 0 \tag{4.1}$$

$$u_c(t_{0+}) = u_c(t_{0-}) = u_c(t_0) = 0 \tag{4.2}$$

where t_{0-} denotes the instant prior to closing the AC circuit breaker, while t_{0+} denotes the instant following closing the AC circuit breaker.

According to Kirchhoff's voltage law (KVL), we have

$$u_R + u_L + u_C = U_0 \tag{4.3}$$

where $u_R = R_{eq} \cdot i$, $u_L = L_{eq} \dfrac{di}{dt}$

Hence, substituting into (4.3), we have

$$R_{eq} \cdot i + L_{eq} \frac{di}{dt} + u_C = U_0 \tag{4.4}$$

Since $i = C_{eq} \dfrac{du_c}{dt}$, (4.4) can be updated to

$$L_{eq} C_{eq} \frac{d^2 u_C}{dt^2} + R_{eq} C_{eq} \frac{du_C}{dt} + u_C = U_0 \tag{4.5}$$

The expression of $u_c(t)$ can be obtained according to the solution of its zero-state response as

$$u_C = A_1 e^{p_1 t} + A_2 e^{p_2 t} + U_0 \tag{4.6}$$

where p_1 and p_2 are the roots of equation (4.5); A_1 and A_2 are the coefficients which can be obtained according to the circuit initial state (4.1) and (4.2),

$$p_{1,2} = -\frac{R_{eq}}{2L_{eq}} \pm \sqrt{(\frac{R_{eq}}{2L_{eq}})^2 - \frac{1}{L_{eq} C_{eq}}}, \; A_1 = -\frac{p_2 U_0}{p_2 - p_1}, \; A_2 = \frac{p_1 U_0}{p_2 - p_1}$$

Therefore, when the circuit reaches the steady-state, the voltage on C_{eq} will be

$$u_C(t_\infty) = U_0 \tag{4.7}$$

Hence, the steady-state voltage of each SM capacitor of the MMC connected with an active AC network before deblocking of the MMC is

$$\frac{u_c(t_\infty)}{n} = \frac{U_0}{n} = \frac{\hat{u}_l}{n} \tag{4.8}$$

According to the system parameters shown in Appendix A, we have

$$\frac{u_c(t_\infty)}{n} = \frac{\hat{u}_l}{n} = \frac{V_{TF2,RMS} \cdot \sqrt{3} \cdot \sqrt{2}}{n} = \frac{30 \cdot \sqrt{3} \cdot \sqrt{2}}{6} = 12.25 \text{ kV} \tag{4.9}$$

where $V_{TF2,RMS}$ is the RMS voltage at the secondary side of the AC transformer.

4.2.2 After the Deblocking of the MMCs

After deblocking the MMC, the SMs on the converter arms are equivalent to controllable voltage sources as shown in Figure 4-5 [133].

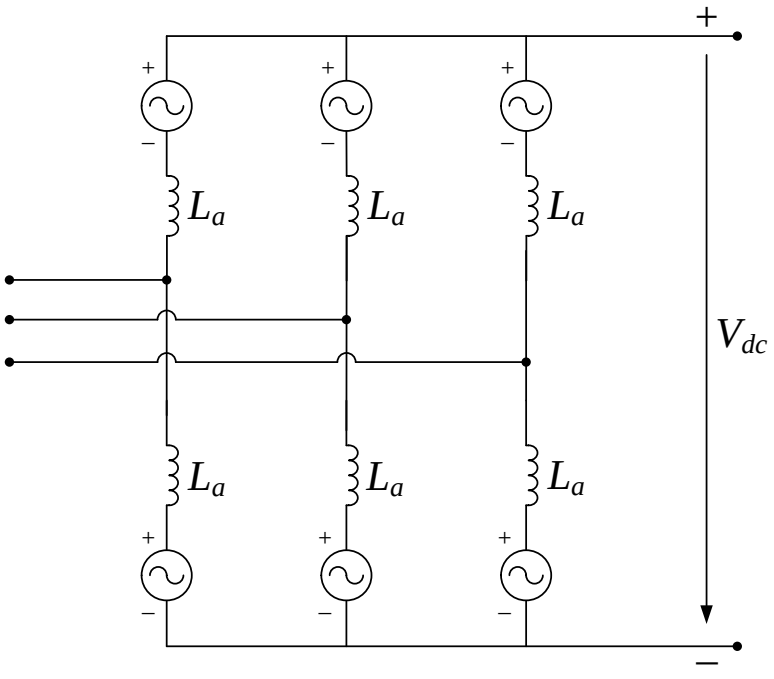


Figure 4-5 Equivalent representation of the SMs in an MMC after deblocking [133]

When the system reaches the nominal condition, the DC voltage is stabilised at V_{dc} and the capacitor voltage of each SM is equally distributed to V_{dc}/n. The capacitor voltage change of a SM from the initial state to the steady-state is illustrated in Figure 4-6 [133].

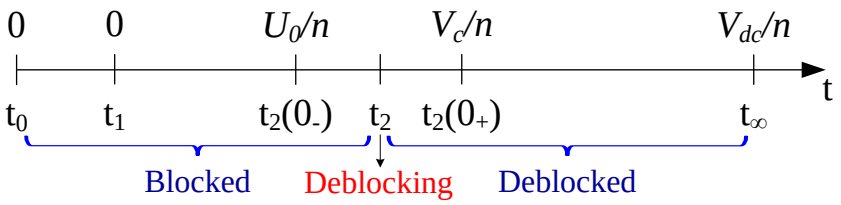


Figure 4-6 Voltage change of a SM from the initial state to the steady-state [133]

During the start-up process, the most significant voltage spikes and current surges emerge at t_2 when the MMC is deblocked. This is because of the voltage difference at the instant before and after t_2. In order to alleviate this impact, one ideal solution is to reduce the voltage difference to zero, so as to achieve the deblocking action at zero voltage difference. Therefore, the reference DC voltage, V_c, at $t_2(0_+)$ should be set to U_0 instead of V_{dc}. However, after deblocking the MMC, the voltage at the MMC AC-side and DC-side has the following mathematical relationship [134]:

$$V_{tabc} = \frac{V_{dc}}{2} \cdot M \tag{4.10}$$

where V_{tabc} is the magnitude of the phase voltage, M is the modulation index.

Generally, the operating range of M is between 0 to 1. Hence, after deblocking the MMC, the minimum controlled DC voltage, V_{dcmin}, is when M = 1. According to (4.10), V_{dcmin} can be obtained as

$$V_{dc\min} = 2 \cdot V_{tabc} \tag{4.11}$$

According to the system parameters shown in Appendix A, we have

$$V_{dc\min} = 2 \cdot V_{tabc} = 2 \cdot V_{TF2,RMS} \cdot \sqrt{2} = 2 \cdot 30 \cdot \sqrt{2} = 84.85 \text{ kV} \tag{4.12}$$

Thus, the minimum SM capacitor voltage is

$$V_{SM\min} = \frac{V_{dc\min}}{n} = \frac{84.85}{6} = 14.14 \text{ kV} \tag{4.13}$$

However, according to the analysis in the previous section and calculation in equation (4.9), the final voltage of the SM capacitor before deblocking the MMC is 12.25 kV.

Since the minimum SM capacitor voltage after deblocking the MMC is larger than the final SM capacitor voltage before deblocking the MMC, zero voltage difference at deblocking the MMC cannot be achieved. However, the zero voltage difference may be achieved with a different design of the system parameters. In order to minimise the impact at the deblocking instant, the DC voltage reference at $t_2(0_+)$ is set to V_{dcmin}.

4.2.3 Hierarchical Start-Up Control Scheme

For the terminals with active AC networks, the master terminal is firstly started to establish the DC voltage, while the slave terminals will be sequentially started afterwards, the procedures of which are named as hierarchical start-up control. Figure 4-7 illustrates the hierarchical start-up control.

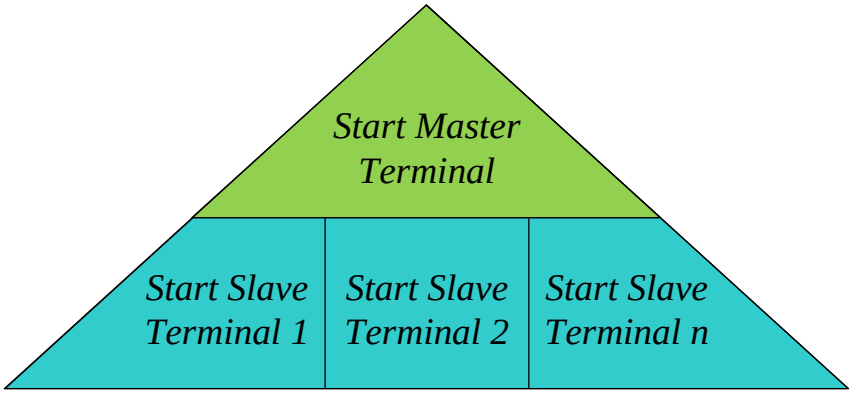


Figure 4-7 Hierarchical start-up control of the terminals with active AC networks

For the start-up control of the master terminal, T2, the DC voltage reference is set to the minimum controlled value V_{dcmin} instead of setting at the nominal value before deblocking MMC-2. It will be increased to the nominal value V_{dc} afterwards when the DC voltage is stably controlled at V_{dcmin}, i.e. not only each terminal is controlled hierarchically, but the DC voltage is also hierarchically regulated. According to the previous analysis, a hierarchical start-up control scheme is proposed for T2 as shown in Table 4-1 [133]:

Table 4-1 Hierarchical Start-Up Control Scheme for the Master Terminal T2 [133]

Step n	**Description**
Step 0	Set the initial DC voltage reference to V_{dcmin};
Step 1	At t_1, close the AC circuit breaker and charge the SM capacitor voltage to U_0/n;
Step 2	At t_2, when the DC voltage is stabilised at U_0, deblock the MMC;
Step 3	When the DC voltage is stably controlled at V_{dcmin}, ramp the DC voltage reference to the nominal value, V_{dc}, to complete the start-up control of this terminal.

For the terminals with active power control, T3 and T4, out of the same purpose of reducing the voltage difference at deblocking the MMC, both MMCs are deblocked when the DC voltage is stably controlled at V_{dcmin} after deblocking MMC-2. Considering the DC voltage at a low level, for the sake of preventing DC overcurrents and reducing the power oscillations,

the power references of both terminals are initially set to 0. Synthesising the start-up control scheme of T2, a comprehensive hierarchical start-up control scheme for the active AC network connected terminals is proposed as shown in Table 4-2:

Table 4-2 Hierarchical Start-Up Control Scheme for the Terminals with Active AC Networks

Step n	Description
Step 0	Set the initial DC voltage reference to V_{dcmin} and power reference to 0;
Step 1	At t_1, close *CB2*;
Step 2	At t_2, when the DC voltage is stabilised at U_0, deblock MMC-2;
Step 3	At t_3, close *CB3*;
Step 4	At t_4, deblock MMC-3;
Step 5	At t_5, close *CB4*;
Step 6	At t_6, deblock MMC-4;
Step 7	At t_5, ramp the DC voltage from V_{dcmin} to the nominal value, V_{dc};
Step 8	At t_6, when the DC voltage is stably controlled at V_{dc}, ramp the power references of MMC-3 and MMC-4 to the nominal values, P_{3ref} and P_{4ref}, in sequence, to complete the start-up control of the terminals with active AC networks;

4.3 Start-Up Process and Control of the Offshore MMC with Passive AC Network

At the initial stage before the system start-up, T1 has neither power output nor AC voltage support. Therefore, it is regarded as a passive AC network. The start-up control of T1 consists of starting the OWF and the MMC. Since the start-up of the OWF requires its terminal voltage being stabilised at the nominal value, the AC voltage at *PCC1* needs to be stabilised. The circuit breaker of the OWF, *CBW*, will not be closed until the voltage at *PCC1* is well

stabilised. For the passive AC network, the voltage at the PCC is established by the control of the MMC. In order to obtain a stable AC voltage at the PCC, the DC-side voltage needs to be well stabilised. Therefore, the start-up control of T1 will not initiate until the DC voltage is stabilised at the nominal state by MMC-2. Based on the above analysis, a basic start-up control sequence can be obtained as follows:

- MMC-2 stabilises the DC voltage to the nominal state;
- Deblock MMC-1 to control the voltage at *PCC1* at nominal state;
- Close *CBW*, deblock the OWF to complete the start-up of T1.

4.3.1 Before the Deblocking of MMC-1

For the passive AC network connected terminal, the AC circuit breaker will not be closed until the voltage at the PCC is stabilised at the nominal state after deblocking the MMC. Hence, before the deblocking of MMC-1, the state of T1 is illustrated in Figure 4-8.

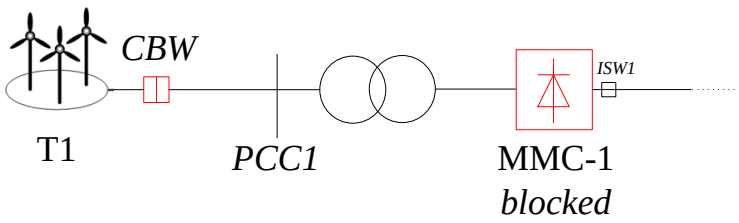


Figure 4-8 State of T1 before the deblocking of MMC-1

A detailed structure of the blocked MMC-1 is depicted in Figure 4-9. Under this condition, the SM capacitors of MMC-1 are initially charged from the DC side. One charging loop is illustrated by the blue dashed line [86], [133].

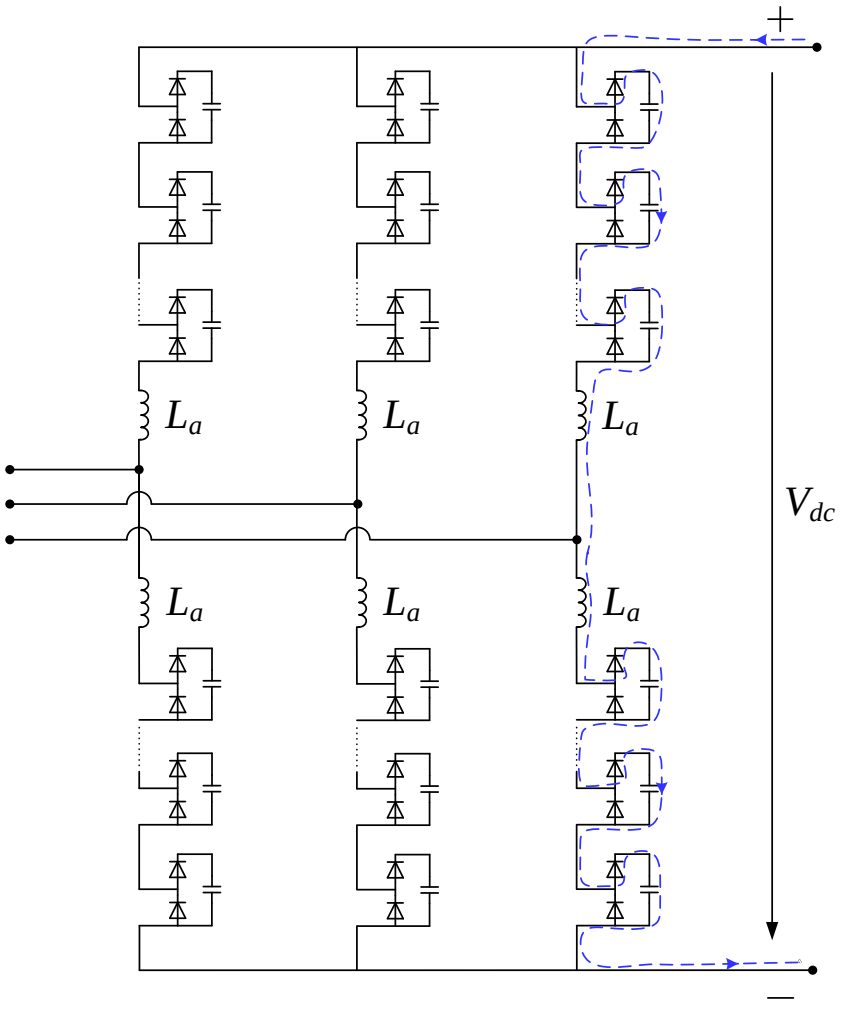
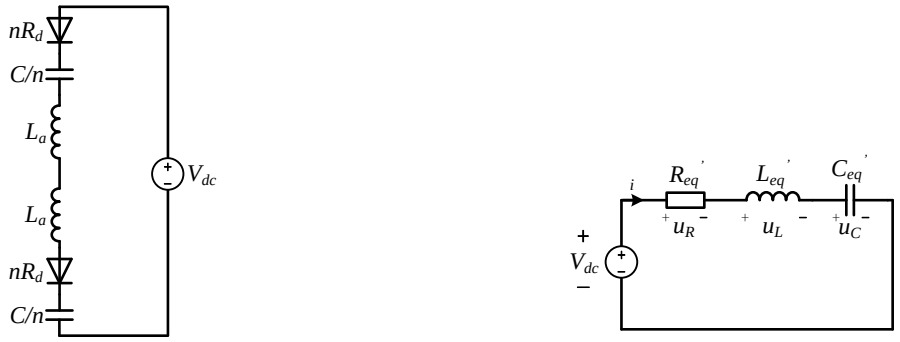


Figure 4-9 Initial charging loop of MMC-1 before deblocking [86], [133]

When the DC voltage is stabilised at the nominal state by MMC-2, considering the losses of the diodes and the circuit resistors, the initial charging loop of the blocked MMC-1 can be represented by a RLC circuit as shown in Figure 4-10(a) where V_{dc} is the nominal DC voltage; L_a is the MMC arm inductance; R_d is the resistance of one diode; C is the capacitance of one SM; n is the number of SMs per arm. It can be further simplified to Figure 4-10(b) where $R_{eq}^{'} = 2nR_d$, $L_{eq}^{'} = 2L_a$, $C_{eq}^{'} = C/2n$.



(a) (b)

Figure 4-10 Equivalent circuit before deblocking MMC-1: (a) equivalent circuit, (b) simplified circuit

Figure 4-3(b) and Figure 4-10(b) are the same 2nd order RLC circuit with the only difference of U_0 being replaced by V_{dc}. According to KVL, we have

$$L_{eq}C_{eq}\frac{d^2u_C}{dt^2}+R_{eq}C_{eq}\frac{du_C}{dt}+u_C=V_{dc} \tag{4.14}$$

According to the mathematical derivation in Section 4.2.1, the solution of (4.14) is

$$u_C=A_1e^{p_1t}+A_2e^{p_2t}+V_{dc} \tag{4.15}$$

The final voltage of the equivalent capacitor at steady-state is

$$u_C(t_\infty)=V_{dc} \tag{4.16}$$

Since there are 2n SMs, the steady-state voltage of each SM capacitor before deblocking MMC-1 is

$$\frac{u_c(t_\infty)}{2n}=\frac{V_{dc}}{2n}=\frac{100}{2\cdot 6}=8.33\ \text{kV} \tag{4.17}$$

4.3.2 After the Deblocking of MMC-1

After deblocking MMC-1, the SM capacitor will finally be charged to V_{dc}/n. The voltage change of the SM capacitor from the initial state is illustrated in Figure 4-11.

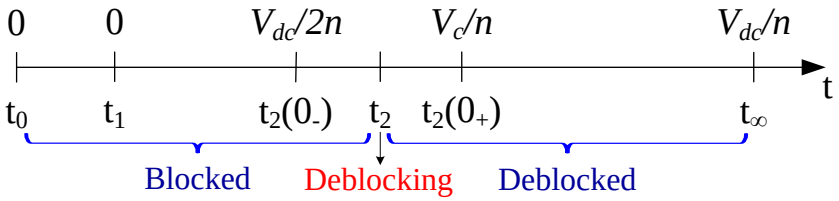


Figure 4-11 Capacitor voltage change of a SM

According to the analysis in Section 4.2.2, the larger voltage difference between $t_2(0_-)$ and $t_2(0_+)$, the more voltage spikes and current surges will emerge at the instant of deblocking the MMC, t_2. In order to reduce the impact, it is expected that the value of V_c could close to $V_{dc}/2$. Therefore, instead of deblocking MMC-1 when the DC voltage is V_{dc}, MMC-1 is deblocked at a reduced DC voltage, which is named as "start-up control scheme with reduced DC voltage". With a different design of the system parameters, the DC voltage may be reduced to $V_{dc}/2$, so that zero voltage difference at deblocking MMC-1 will be achieved and the scheme can be named as "start-up control scheme with half DC voltage". According to (4.12), the minimum DC voltage, $V_{dc\min}$, can be controlled to 84.85 kV and cannot be controlled to $V_{dc}/2$. The start-up control scheme for the offshore connected terminal is shown in Table 4-3:

Table 4-3 Start-Up Control Scheme for the Terminal with OWF

Step n	**Description**
Step 0	Set the initial AC voltage reference of MMC-1 to 0, wait until MMC-2 stabilises the DC voltage to V_{dc};

Step 1	At t_1, when the SM capacitor voltage is charged to $V_{dc}/2n$, reduce the DC voltage reference of T2 to $V_{dc\min}$;
Step 2	At t_2, when the DC voltage is stabilised at $V_{dc\min}$, deblock the MMC-1;
Step 3	At t_3, ramp the DC voltage reference back to the nominal value, V_{dc};
Step 4	At t_4, when the DC voltage is stably controlled at V_{dc}, ramp the AC voltage reference to the nominal value, V_{ac};
Step 5	At t_5, when the voltage at *PCC1* is well stabilised at V_{ac}, close *CBW* and then deblock the OWF to complete the start-up control of the offshore terminal.

4.3.3 Comprehensive Start-Up Control Sequence

Synthesising the start-up control of both the active and passive AC networks connected terminals, a comprehensive start-up control scheme is proposed as shown in Table 4-4:

Table 4-4 Comprehensive Start-Up Control Scheme for the Offshore Integrated MMC MTDC

Step n (t_n)	**Description**
Step 0 (t_0)	Initially, set DC voltage reference of MMC-2 to V_{dcmin}, AC voltage reference of MMC-1 to 0, power references of both MMC-3 and MMC-4 to 0;
Step 1 (t_1)	Close *CB2*;
Step 2 (t_2)	When the DC voltage reaches U_0, deblock MMC-2;
Step 3 (t_3)	Close *CB3*;
Step 4 (t_4)	Deblock MMC-3;
Step 5 (t_5)	Close *CB4*;
Step 6 (t_6)	Deblock MMC-4;
Step 7 (t_7)	When the DC voltage is stabilised at V_{dcmin}, ramp the DC voltage reference to the nominal value V_{dc};
Step 8 (t_8)	When the DC voltage is stabilised at V_{dc}, reduce the DC voltage reference to V_{dcmin};

Step 9 (t_9)	Deblock MMC-1;
Step 10 (t_{10})	When the DC voltage is stabilised at V_{dcmin}, ramp the DC voltage reference to the nominal value, V_{dc};
Step 11 (t_{11})	When the DC voltage is stabilized at V_{dc}, ramp the AC voltage reference of MMC-1 to the nominal value, V_{ac};
Step 12 (t_{12})	Ramp the active power reference of MMC-4 to the nominal value, P_{4ref}^*;
Step 13 (t_{13})	Ramp the active power reference of MMC-3 to the nominal value, P_{3ref}^*;
Step 14 (t_{14})	When the voltage at *PCC1* is well stabilised at V_{ac}, close *CBW*;
Step 15 (t_{15})	Deblock the OWF and complete the start-up control of the system.

During the start-up process, the master terminal T2 with DC voltage control is started to initially charge the SM capacitors of MMC-2, the DC grid, and the SM capacitors of the other 3 MMCs. Then T3 and T4 are started in sequence with the DC voltage maintained at the minimum value, V_{dcmin}, so as to minimise the voltage difference of the SM capacitors before and after the deblocking operation. Meanwhile, the active power references of MMC-3 and MMC-4 are not increased to the nominal values at this point. This is because 1) the DC voltage has not been stabilised at the nominal value; 2) the deblocking of MMC-1 will lead to voltage and current oscillations, both power references will not be increased to the nominal values until the deblocking of MMC-1. If both power references are kept at 0, the current will oscillate around 0. However, if both power references are increased to the nominal state before the deblocking of MMC-1, the current will oscillate around their nominal values, which has more possibility of emerging overcurrent.

In order to deblock MMC-1 with the minimum voltage difference of the SM capacitors, the DC voltage is increased to the nominal value to further charge the SM capacitors in MMC-1 and then decreased to the minimum controlled value before deblocking MMC-1. This control

process is called start-up control with reduced DC voltage. After deblocking MMC-1, the DC voltage is ramped back to the nominal value and then the AC voltage reference of MMC-1 is ramped to control the voltage at *PCC1* to the nominal value for the integration of the OWF. Since the closing of CBW necessitates stable AC terminal voltage, a longer delay is set before this operation and the active power references of MMC-3 and MMC-4 are ramped to the nominal values during the delay. When the OWF is started with stable output power, the start-up of the whole system is completed.

4.4 Simulation Case Studies

In order to evaluate the proposed start-up control scheme, 3 case studies are conducted on the RTDS. In Case A, the system is started using the proposed start-up control sequence in which 1) appropriate changes on the DC voltage reference, including the reduced DC voltage control, are applied; 2) appropriate initial settings on the AC voltage reference of MMC-1, active power reference of MMC-3 and MMC-4, are applied; 3) ramping the reference setting of the AC voltage and active power at appropriate time is applied, to finally complete the start-up of the whole system. In Case B, similar start-up control sequence is used, except that the DC voltage reference is always maintained at the nominal value with neither the initial setting at V_{dcmin} nor using the reduced DC voltage start-up control at the instant of deblocking MMC-1. The start-up control of Case C is similar to that of Case B, except that the references of AC voltage and active power are kept constant at nominal values without changes. A comparison of the start-up control used in 3 cases is presented in Table 4-5.

Table 4-5 Comparison of the Start-Up Control of 3 Cases

Case A	The start-up control sequence with reference settings of V_{dc}, V_{ac}, P_{3ref} and P_{4ref} are the same as proposed in Section 4.3.3;
Case B	The start-up control sequence is the same as that of Case A, except that the reference settings of V_{dc} is always kept constant at the nominal value;
Case C	The start-up control sequence is the same as that of Case B, except that the reference settings of V_{ac}, P_{3ref} and P_{4ref} is always kept constant at the nominal value;

4.4.1 Case A

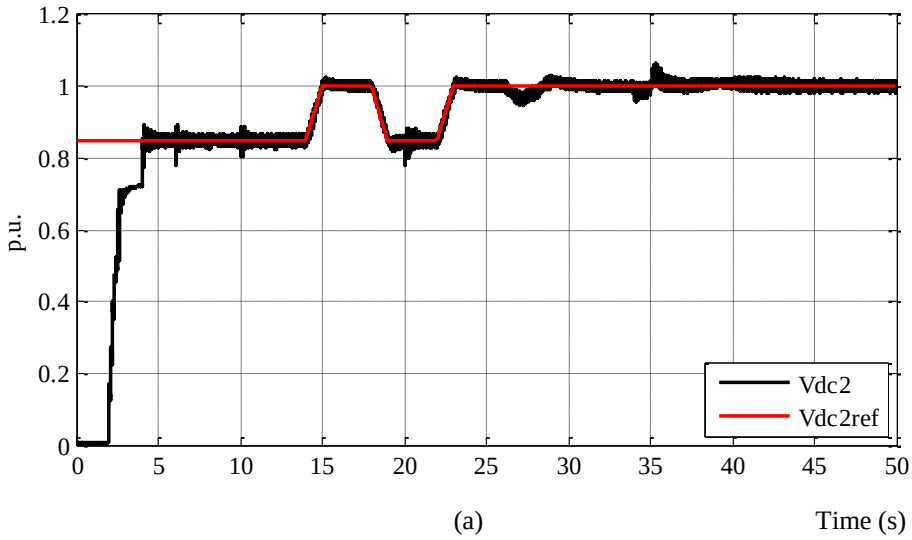
The proposed start-up control sequence is applied in this case. In order to clearly illustrate the system performance with each corresponding control action, Table 4-6 presents the specific time of each control action. The order of the control actions is the main focus of the proposed start-up control, while the time delay between two sequential control actions is not the main focus.

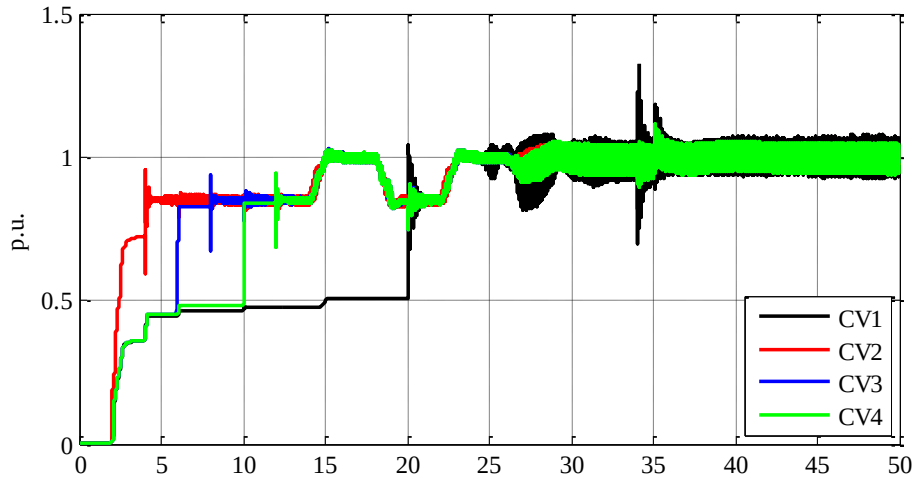
Table 4-6 Description of the Operational Time of the Proposed Control Sequence

t_n	Time	Description	Comment
t_0	0 s	Set $V_{dcref} = V_{dcmin}$, $V_{acref} = 0$, $P_{3ref} = P_{4ref} = 0$	
t_1	2 s	Close *CB2*	A delay of 2 s is set between two sequential control actions. This delay can be shortened as long as the system reaches a steady condition after the former control action.
t_2	4 s	Deblock MMC-2	
t_3	6 s	Close *CB3*	
t_4	8 s	Deblock MMC-3	
t_5	10 s	Close *CB4*	
t_6	12 s	Deblock MMC-4	
t_7	14 s	Set $V_{dcref} = V_{dc}$	
t_8	18 s	Set $V_{dcref} = V_{dcmin}$	A delay of 4 s is set when the DC voltage reference is increased to nominal value. The SM capacitors of

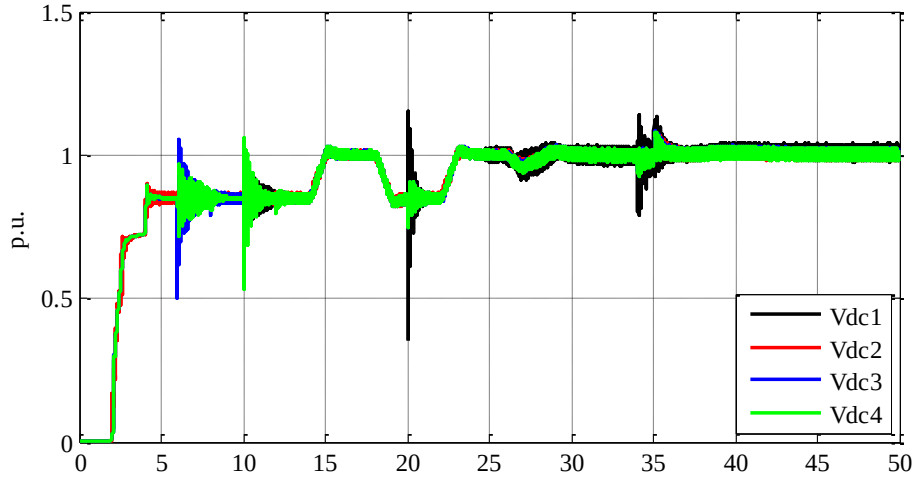
			MMC-1 will be pre-charged from the DC side.
t_9	20 s	Deblock MMC-1	A delay of 2 s is set between two sequential control actions. This delay can be shortened as long as the system reaches a steady condition after the former control action.
t_{10}	22 s	Set $V_{dcref} = V_{dc}$	
t_{11}	24 s	Set $V_{acref} = V_{ac}$	
t_{12}	26 s	Set $P_{4ref} = P_{4ref}^*$	
t_{13}	28 s	Set $P_{3ref} = P_{3ref}^*$	
t_{14}	34 s	Close *CBW*	The re-integration of the OWF needs a stable AC voltage at *PCC1*. Hence, a long delay of 6 s is chosen.
t_{15}	35 s	Deblock OWF and complete start-up control	

The simulation results are demonstrated in Figure 4-12: (a) DC voltage controlled by MMC-2; (b) voltage of one SM capacitor in each MMC; (c) DC voltages of the MTDC; (d) DC currents of the MTDC; (e) MMC AC-side voltages in RMS value; (f) MMC AC-side currents in RMS value; (g) active power; (h) reactive power, where V_{dc2ref} denotes the reference setting of the DC voltage of MMC-2, CV*n* (*n* = 1,…,4) denotes the capacitor voltage of one SM in MMC-*n*.

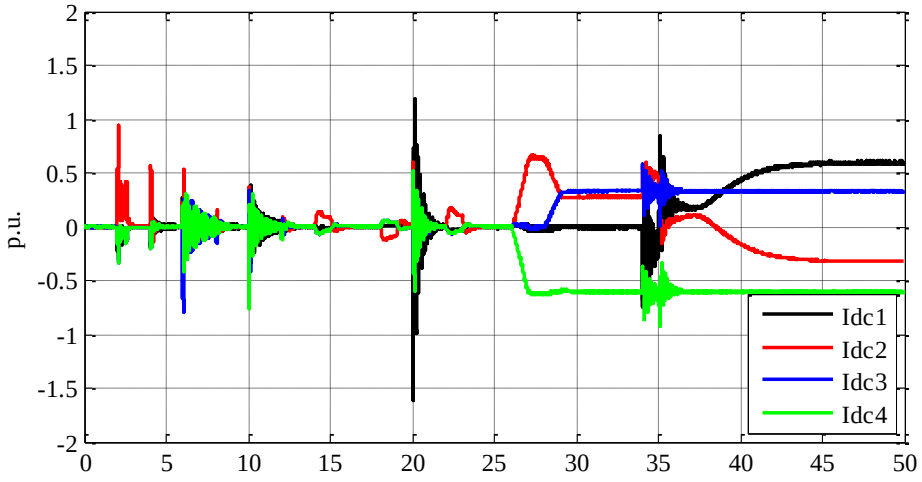




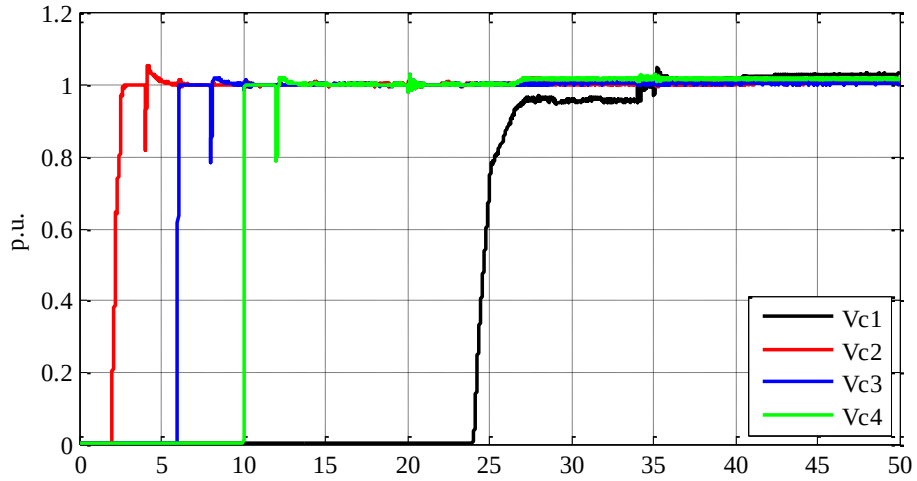
(b) Time (s)



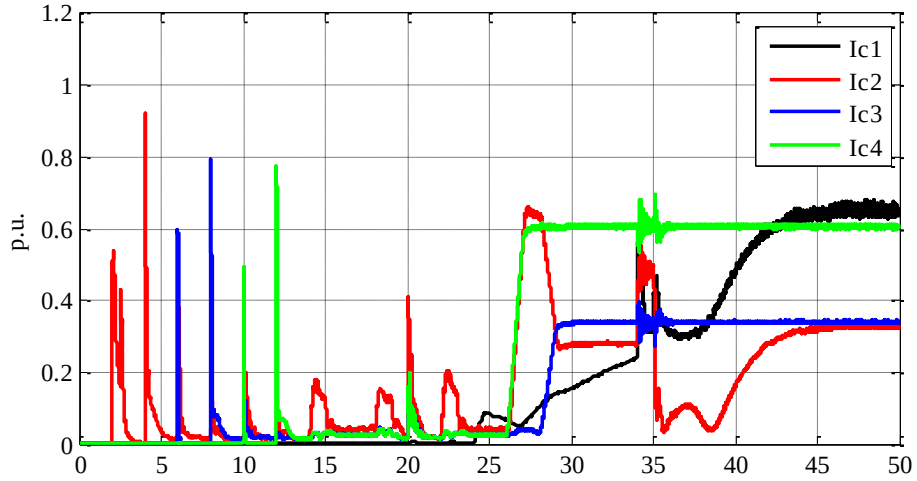
(c) Time (s)



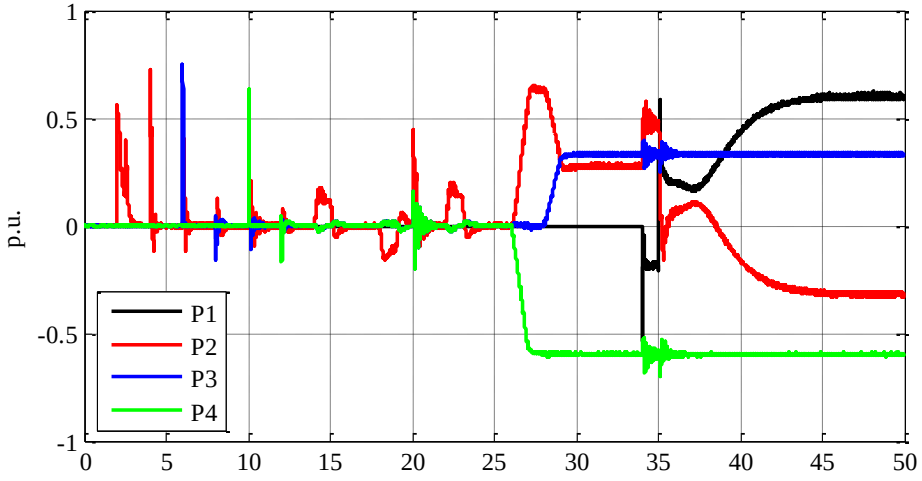
(d) Time (s)



(e) Time (s)



(f) Time (s)



(g) Time (s)

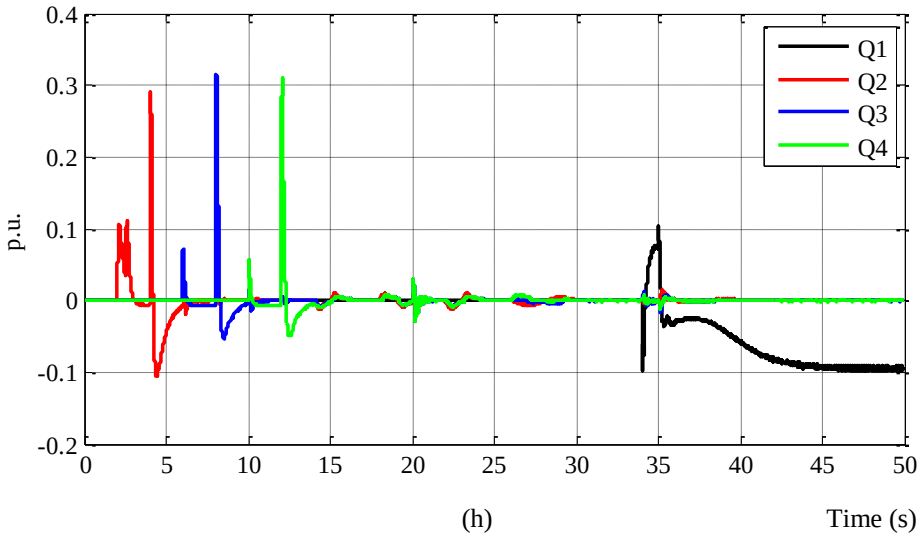


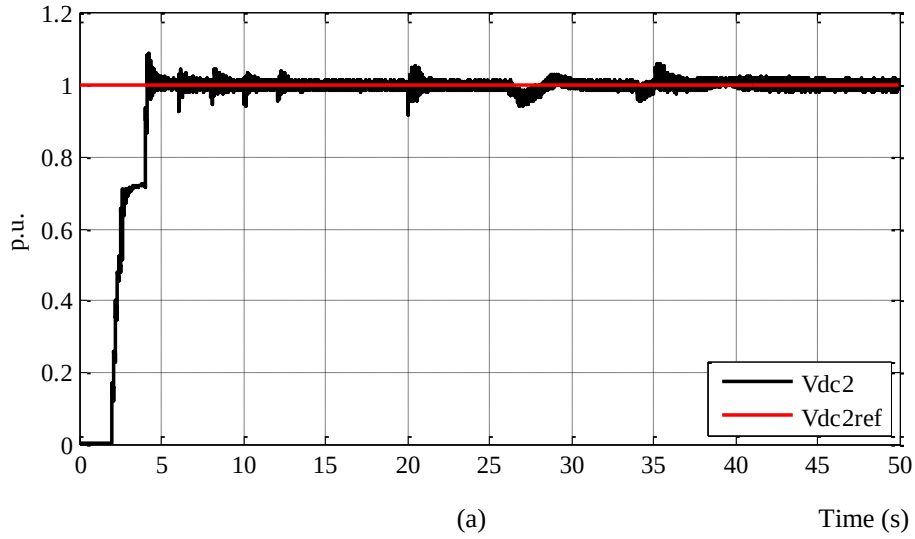
Figure 4-12 System start-up performance using the proposed start-up control sequence

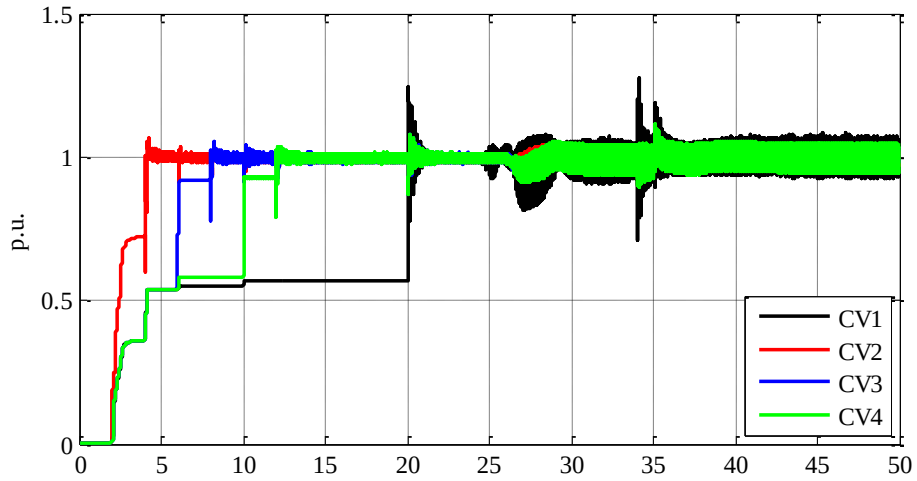
Figure 4-12(a) demonstrates the performance of the DC voltage controlled by MMC-2. Before the deblocking of MMC-2, the DC voltage reference is set at V_{dcmin}. After deblocking MMC-2 at 4 s, the DC voltage reaches V_{dcmin} and well tracks the voltage reference until the end with small oscillations. Figure 4-12(b) presents the performance of the capacitor voltage of one SM in each MMC. At the instant of deblocking each MMC, the capacitor voltage difference of the SM is regulated at the minimum controllable value. Therefore, the voltage oscillations at deblocking the MMC are reduced accordingly. In Figure 4-12(c), the most significant DC voltage spikes emerge at the DC-side of T1 at 20 s when MMC-1 is deblocked as shown in Table 4-6. This is because before deblocking MMC-1, its SM capacitor voltage is $V_{dc}/2$ and after deblocking MMC-1, it becomes V_{dcmin}. This voltage difference, compared with that of the other 3 MMCs at the deblocking instant, is larger, which contributes larger voltage spikes. Due to the same reason, the most significant DC current surges emerge at DC-side of T1 at 20 s as shown in Figure 4-12(d). Figure 4-12(e) shows that the MMC AC-side voltages reach the nominal value in sequence with few oscillations. Figure 4-12(f) shows the performance of the MMC AC-side currents, which reach the nominal values smoothly. Figure 4-12(g) shows the

active power reaches the nominal value with small oscillations. At 30 s, *CBW* is closed and then the OWF is deblocked, the OWF is stably started with smoothly increased output power. Figure 4-12(h) presents small reactive power oscillations during the start-up process. Due to the effective start-up control with reduced DC voltage and appropriate changes on the reference settings, each terminal is stably started in sequence and the system reaches the nominal operating condition with small voltage spikes and current surges.

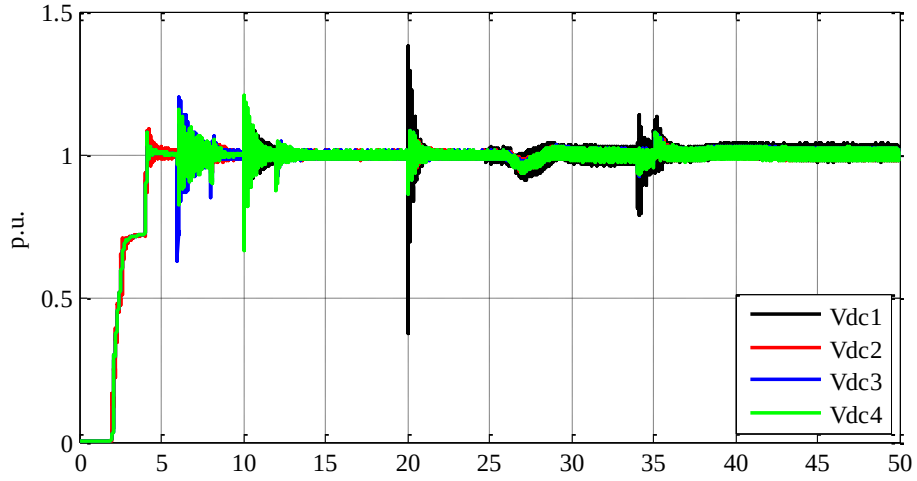
4.4.2 Case B

In this case, the start-up control sequence is the same as that of Case A, except that the DC voltage reference of MMC-2 is always kept at the nominal value. That is, the DC voltage reference is not set at V_{dcmin} at the initial start-up stage and the reduced DC voltage start-up control is not applied during the start-up process. The simulation results are demonstrated in Figure 4-13: (a) DC voltage controlled by MMC-2; (b) voltage of one SM capacitor in each MMC; (c) DC voltages of the MTDC; (d) DC currents of the MTDC; (e) MMC AC-side voltages in RMS value; (f) MMC AC-side currents in RMS value; (g) active power; (h) reactive power.

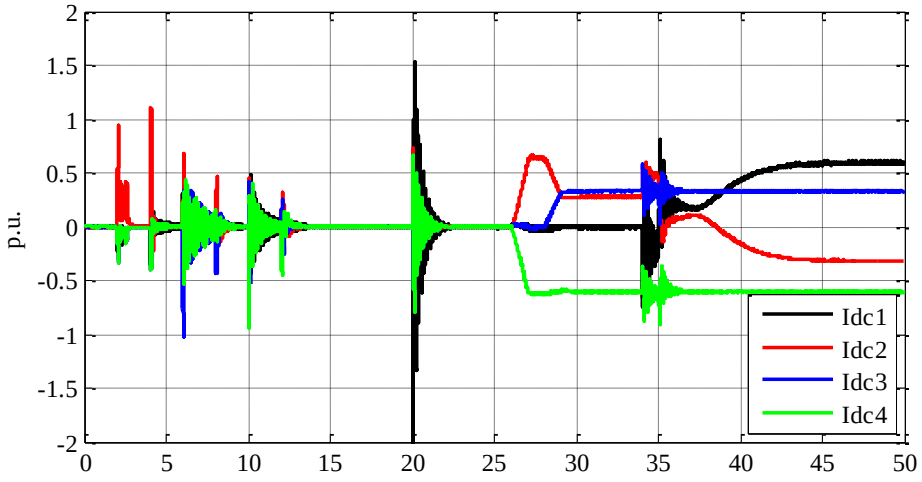




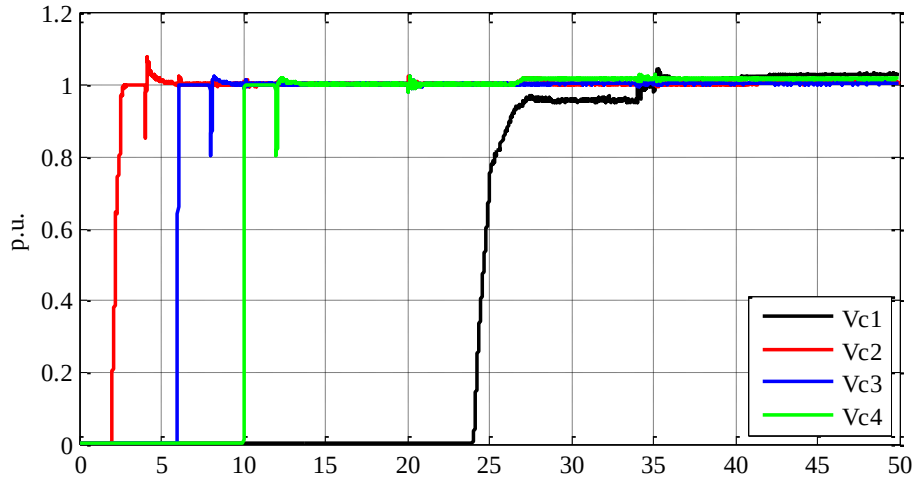
(b) Time (s)



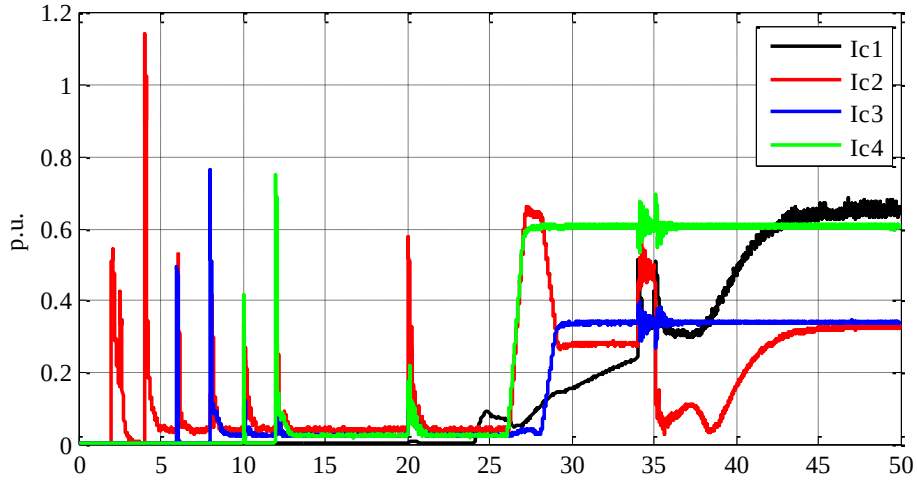
(c) Time (s)



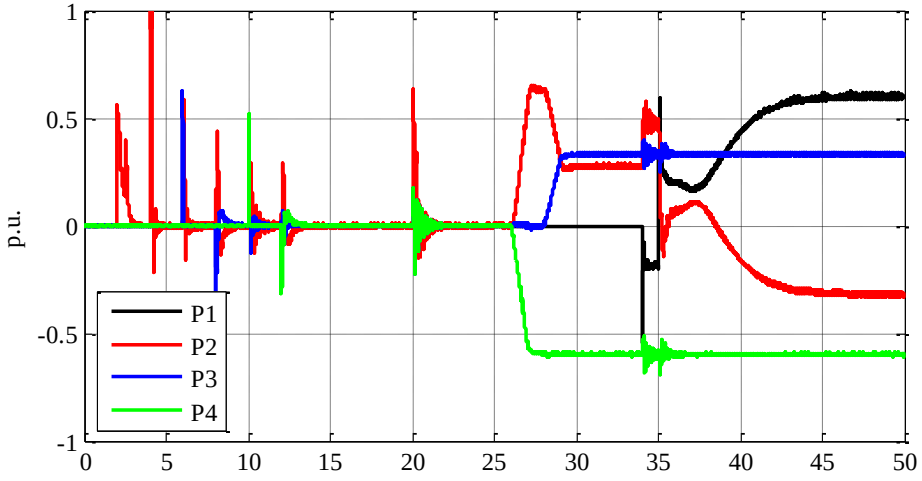
(d) Time (s)



(e) Time (s)



(f) Time (s)



(g) Time (s)

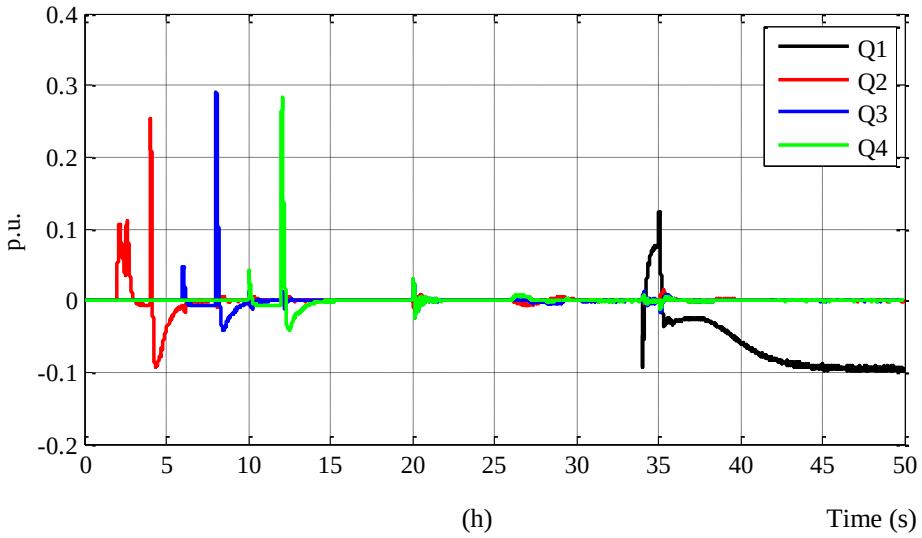
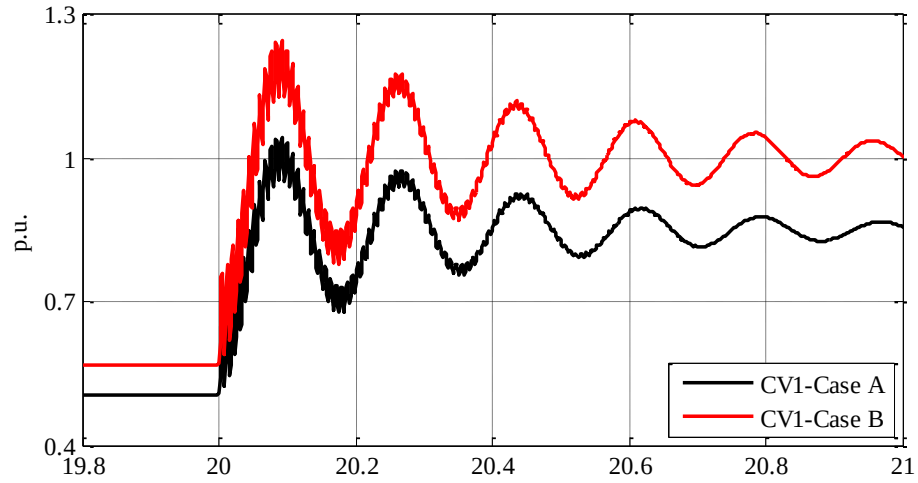


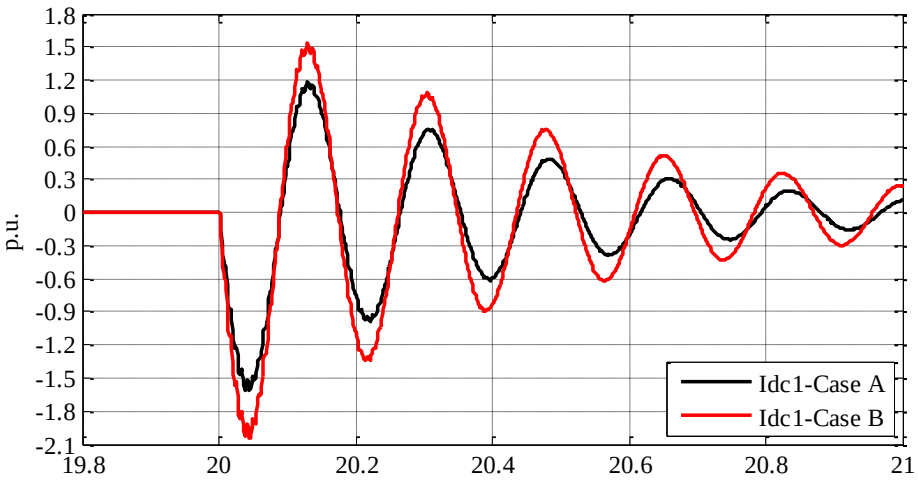
Figure 4-13 System start-up performance using the start-up control sequence without reduced DC voltage control

Since the DC voltage is maintained at the nominal value during the start-up process, the SM capacitor voltage will instantly increase to the nominal value after deblocking of the associated MMC. Before the deblocking of MMC-2, the SM capacitor voltage is U_0/n and it will become V_{dc}/n after deblocking. In Case A, due to the initial setting on the DC voltage, the SM capacitor voltage will become V_{dcmin}/n after deblocking MMC-2, which minimises the voltage different at the deblocking instant and hence reduces the oscillations on the voltage and current. Figure 4-13(c) shows the voltage spikes are larger than those in Case A at 4 s when MMC-2 is deblocked. The DC current surges shown in Figure 4-13(d), MMC AC-side current surges shown in Figure 4-13(f) and the active power oscillations shown in Figure 4-13(g) are more significant than those in Case A at 4 s. Similarly, the voltage differences of the SM capacitors become larger when deblocking MMC-3 and MMC-4 than those in Case A, which leads to more oscillations on the voltages and currents at the deblocking instant. In Figure 4-12(d), there are almost no current surges at 8 s and 12 s when deblocking MMC-3 and MMC-4. However, Figure 4-13(d) shows small current surges at those instants. The

active power oscillations shown in Figure 4-13(g) are apparently larger than those in Case A at 8 s and 12 s. In this case, the reduced DC voltage start-up control is not applied at deblocking MMC-1. Figure 4-13(c) demonstrates the peak of the voltage spikes increase to nearly 1.4 p.u., which is much larger than that in Case A which is less than 1.2 p.u. at 20 s. Figure 4-13(d) presents the peak of the current surges is over 2 p.u. at 20 s, while in Case A it is around 1.6 p.u.. In order to visibly compare the differences of the system performance between Case A and Case B, the performance of the capacitor voltage of MMC-1 and DC current at T1 with a zoomed proportion at 20 s is shown in Figure 4-14.



(a) Time (s)



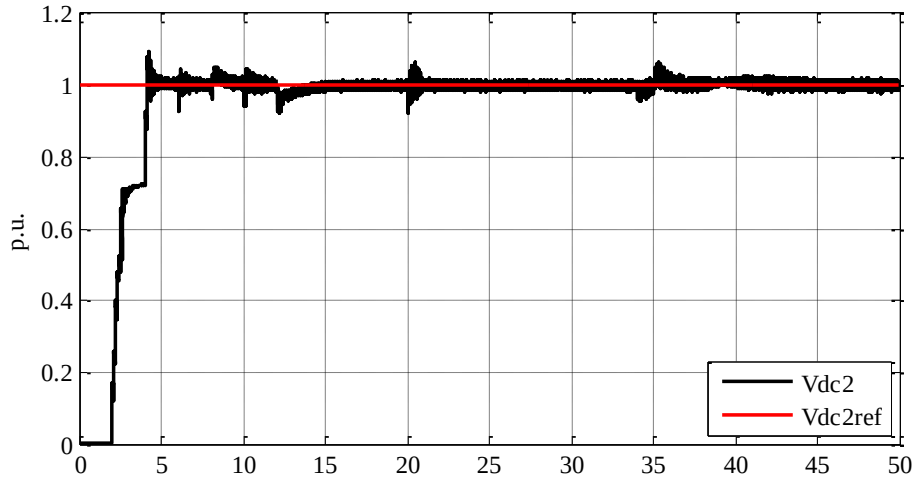
(b) Time (s)

Figure 4-14 Comparison of the system start-up performance of Case A and Case B: (a) Capacitor voltage of MMC-1; (b) DC current at T1

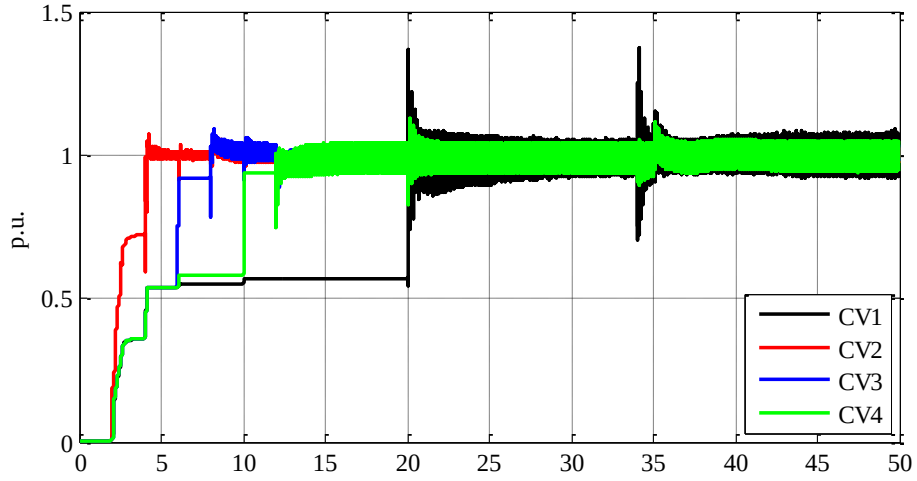
In Figure 4-14(a), the peak capacitor voltage in Case A is 1.05 p.u. which is 20% smaller than that in Case B. In Figure 4-14(b), the peak DC current at T1 in Case A is 1.5 p.u. which is 25% smaller than that in Case B. Hence, the voltage spikes of the capacitor voltages and DC current surges in Case B when deblocking the MMCs are more significant than those in Case A, which is due to the fact that the DC voltage is not appropriately adjusted.

4.4.3 Case C

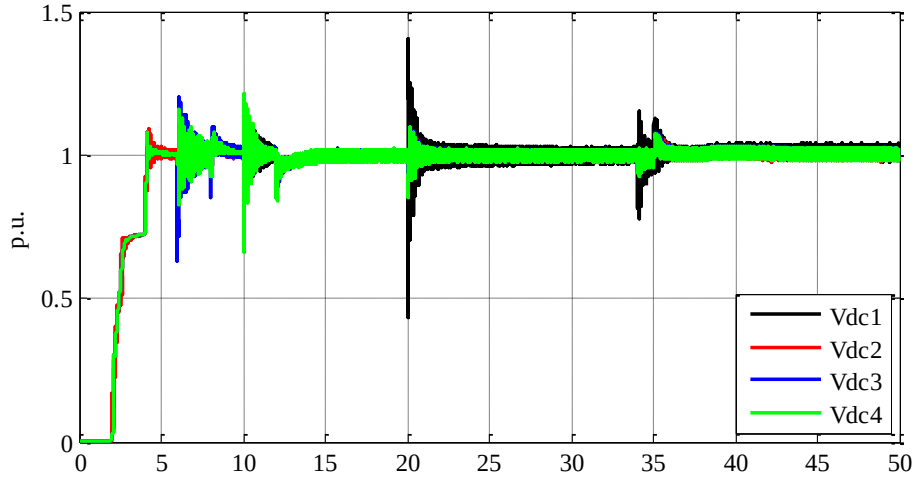
In this case, not only the DC voltage reference of MMC-2 is kept at the nominal value, but the AC voltage reference of MMC-1, active power references of MMC-3 and MMC-4 are also kept at their nominal values without change during the start-up process. The simulation results are demonstrated in Figure 4-15: (a) DC voltage controlled by MMC-2; (b) voltage of one SM capacitor in each MMC; (c) DC voltages of the MTDC; (d) DC currents of the MTDC; (e) MMC AC-side voltages in RMS value; (f) MMC AC-side currents in RMS value; (g) active power; (h) reactive power.



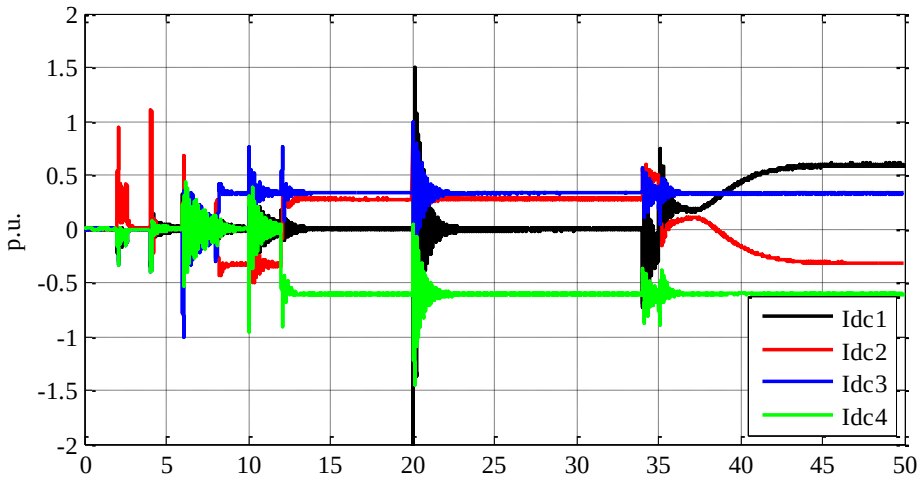
(a) Time (s)



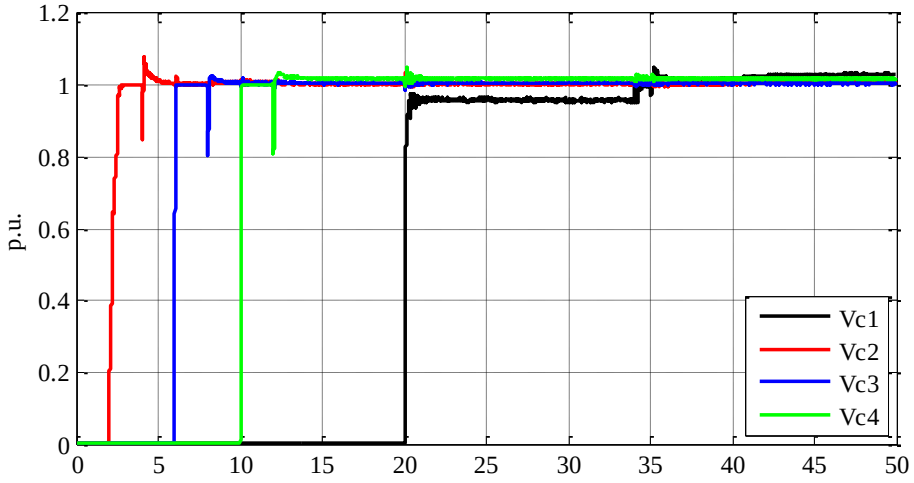
(b) Time (s)



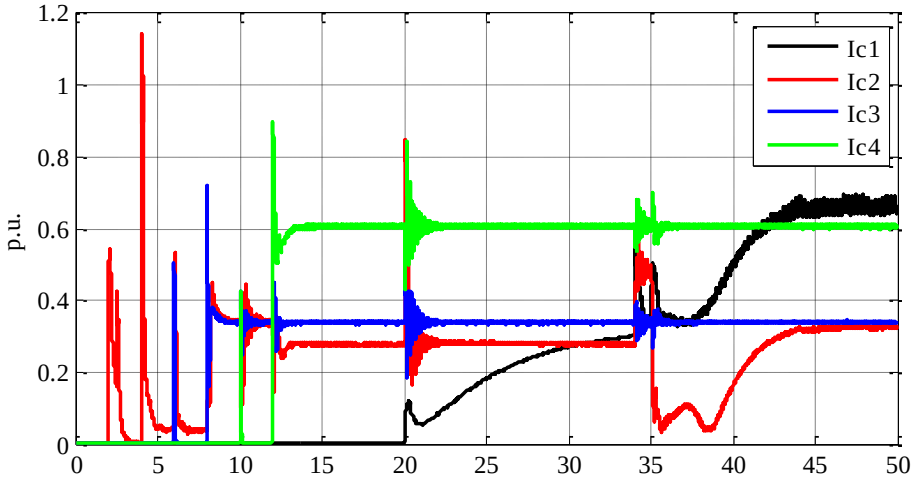
(c) Time (s)


p.u.
Idc1
Idc2
Idc3
Idc4
Time (s)

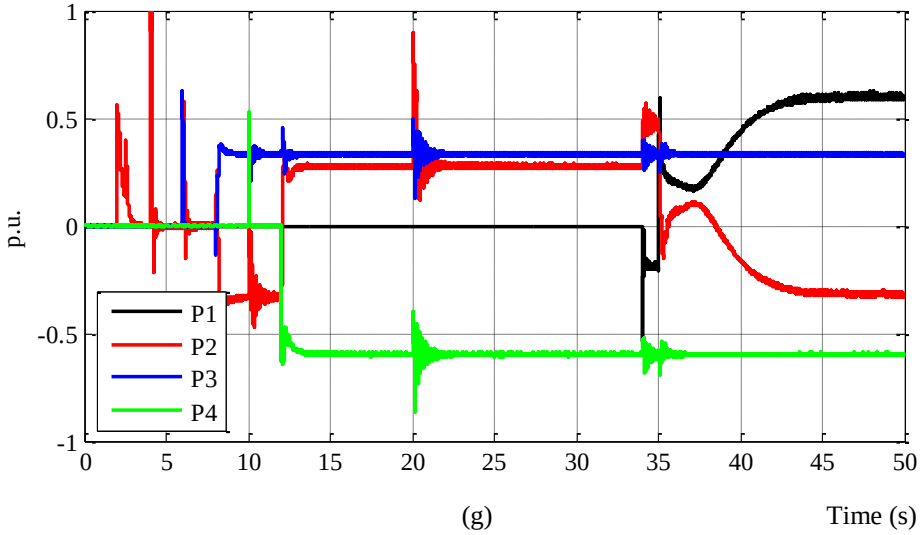
(d)


p.u.
Vc1
Vc2
Vc3
Vc4
Time (s)

(e)


p.u.
Ic1
Ic2
Ic3
Ic4
Time (s)

(f)



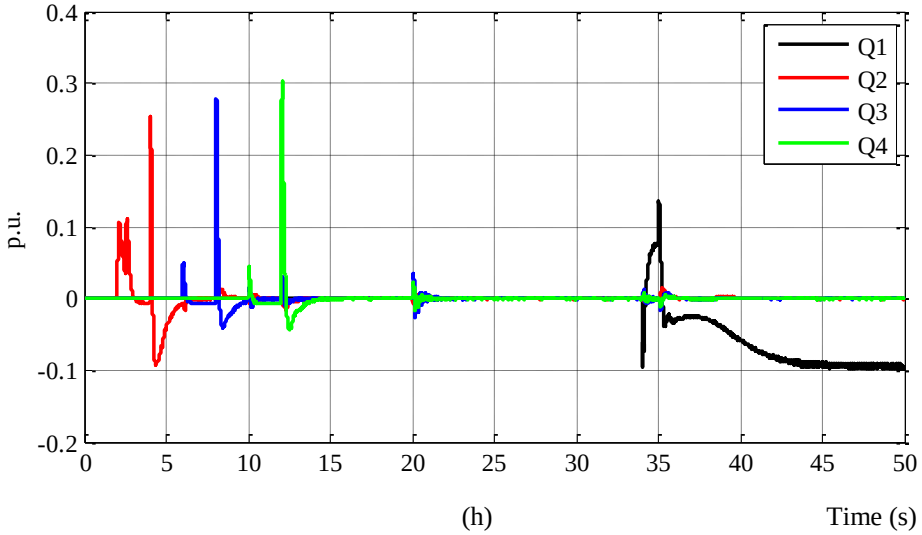


Figure 4-15 System start-up performance using the start-up control sequence without any changes on the voltage and power settings

Similar to Case B, since the DC voltage reference is not set at V_{dcmin} when deblocking MMC-2, larger voltage spikes and current surges can be observed at 4 s in Figure 4-15(c), (d) and (f) in comparison with those in Case A. Since the active power references of MMC-3 and MMC-4 are kept at the nominal values at the beginning, the active power has been stably transferred from both terminals before the deblocking of MMC-1. When MMC-1 is deblocked at 20 s, voltage and current oscillations will emerge. In the previous 2 cases, since the active power

references of MMC-3 and MMC-4 are initially maintained at 0, the currents of both terminals are stabilised at 0 before deblocking MMC-1 and will oscillate around 0 after deblocking MMC-1. However, in this case, since both terminals are transferring power before deblocking MMC-1, the current will oscillate around its nominal value, which has more possibilities for the current oscillating over the limit. In Case A and Case B, the largest DC current oscillations emerge at T1 and has proportions over the predefined rating, while the DC current oscillations at other 3 terminals do not exceed it after deblocking MMC-1 at 20 s. However, in Case C, the DC current oscillations at T1, T3 and T4 all exceed the predefined rating after deblocking MMC-1 at 20 s as shown in Figure 4-15(d). In Figure 4-15(f), although the AC current oscillations at the MMC AC-side do not generate overcurrent, the oscillations at T4 have potential risk due to it oscillates around the nominal value instead of 0. Figure 4-15(g) demonstrates the peak value of the active power oscillations at 20 s is more significant than those in Case A and Case B. Therefore, based on the analysis and comparisons of the 3 cases, it is suggested to provide initial settings for the voltage and power references and ramp them to the nominal value at the appropriate instant, which reduces the possibility of the emergence of overvoltages and overcurrents and improves the system start-up performance in a more stable manner.

4.4.4 Discussion and Comparison of the 3 Cases

Case A applies the proposed start-up control scheme. Due to the appropriate control sequence with appropriate initial settings and adjustment on the reference of the DC voltage, AC voltage, and active power, the system has been stably started with small voltage spikes and current surges. In Case B, the DC voltage is kept at the nominal value without reduced DC voltage control during the start-up process, larger voltage spikes and current surges have been

observed after deblocking the MMCs. In Case C, the references of DC voltage, AC voltage, and active power are all kept at the nominal values without initial settings, similar oscillations to those in Case B can be observed after deblocking the MMCs. In addition, DC overcurrents at T1, T3 and T4 have been identified after deblocking MMC-1, while in Case A and Case B, only T1 has overcurrent. Meanwhile, the MMC AC-side current at T4 has a potential risk of overcurrent. Therefore, in comparison of the 3 cases, the proposed start-up control scheme in Case A has demonstrated superiority in the system start-up. Table 4-7 presents the comparison of the start-up control performance of the 3 cases.

Table 4-7 Comparison of the Start-Up Control Performance of 3 Cases

Case A	System is stably started with small voltage spikes and current surges. The only overcurrent emerges at T1 at around 20 s after deblocking MMC-1;
Case B	System is stably started with more voltage spikes and current surges than those in Case A. More voltage spikes and current surges emerge after deblocking the MMCs and larger overcurrent emerges at T1 at around 20 s after deblocking MMC-1;
Case C	System is stably started with similar voltage spikes and current surges to those in Case B. Overcurrent emerges at T1, T3 and T4 at around 20 s after deblocking MMC-1. T4 has potential risk of occurring MMC AC-side overcurrent after deblocking MMC-1.

Although the start-up performance of Case C seems the worst, due to appropriate start-up sequence applied, the start-up performance has been stable. If all terminals are started randomly or simultaneously, it may lead to unstable start-up of the OWF, failure of the OWF integration or even the whole system collapse.

4.5 Summary

In this chapter, the system start-up control has been investigated. According to the characteristics of the AC networks that connect with the MTDC, the system terminals have been categorised into the onshore terminals with active AC networks and the offshore terminal in which the OWF is regarded as a passive AC network before the start-up. For the onshore terminals, the mathematical models before and after the deblocking of the MMC have been derived and a hierarchical start-up control scheme has been proposed. For the offshore terminal, the mathematical models before and after the deblocking of the MMC have also been derived and a reduced DC voltage control scheme has been proposed for the start-up of the terminal with passive AC network. Combining the start-up control of the onshore and offshore terminals, a comprehensive start-up control scheme for the whole system has been proposed. Although zero voltage difference is not achieved at deblocking the MMCs, the proposed start-up control scheme achieves minimum voltage difference on SMs when deblocking the MMCs.

To evaluate the proposed start-up control scheme, 3 case studies have been conducted using RTDS simulations. Based on the analysis and simulation results, 3 conclusions have been drawn as follows:

- Since effective start-up control of each terminal in sequence has been applied in all 3 cases instead of starting the terminals randomly or starting all terminals simultaneously, the system was started in a stable manner using the start-up sequence in each case;

- Appropriate initial setting and adjustment on the controlled DC voltage is important and can minimise the voltage difference of the SM capacitor at the instant of deblocking the MMC, which contributes to small voltage spikes and current surges when deblocking the MMCs ;
- Initial settings of the AC voltage and active power and ramp them at the appropriate instant is important. They can reduce the possibility of the emergence of the overvoltages and overcurrents during the start-up process.

CHAPTER 5 CONTROL AND PROTECTION OF THE MMC MTDC SYSTEM WITH AN OWF AGAINST AC FAULTS

Faults, including AC or DC faults, may occur on real power systems. Hence control and protection against faults is essential. This chapter aims to investigate control and protection under AC fault conditions. The objectives of this chapter are: 1) to study the system fault characteristics under a three-phase to ground fault at different locations; 2) to propose corresponding control and protection strategy against the fault according to the fault characteristics; 3) to identify the emergency condition that the system may experience and the potential risks that may exist after the fault occurs; 4) to propose special control and protection under the emergency condition.

5.1 Introduction

5.1.1 General Control and Protection and Some Definitions

Generally, a comprehensive process of control and protection against a fault consists of [35], [135]-[136]: Phase 1) fault detection; Phase 2) fault location; Phase 3) fault isolation; Phase 4) faulted section isolation; Phase 5) system recovery, as illustrated in Figure 5-1.

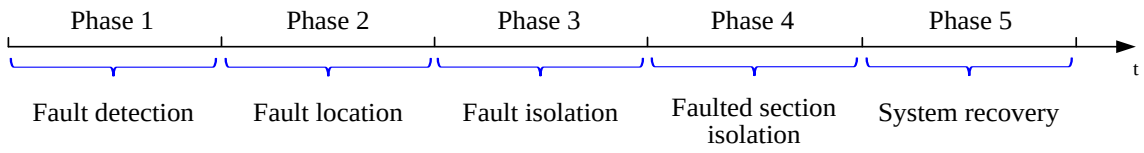


Figure 5-1 Comprehensive process of control and protection against a fault

where each phase is defined as follows:

- **Phase 1) Fault detection**: According to the system fault characteristics such as low voltage or overcurrent, to confirm the fault existence;
- **Phase 2) Fault location**: According to the fault characteristics such as change of current direction or impedance, to locate the fault position;
- **Phase 3) Fault isolation**: After locating the fault, apply associate control and protection action to speedily isolate the fault, so as to reduce the impact on the system and finally prevent current injecting into the faulted point;
- **Phase 4) Faulted section isolation**: Open/trip the mechanical switch between the faulted point to physically isolate the faulted line section;
- **Phase 5) System recovery**: Resume the unfaulted sections of the system.

For the sake of clarity, some of the frequent expressions in this chapter and the next chapter are defined here [137]:

- **Control mode**: Defines the converter level control under steady-state condition, such as DC voltage/AC voltage control, active/reactive power control, as described in Section 2.3.3;
- **Control and protection strategy**: Defines control and protection actions after a fault occurs, such as block/deblock the MMC, trip/reclose the AC circuit breaker, open/close the DC *ISW*;
- **Control and protection sequence**: Defines the order of control and protection actions in control and protection strategy and the delay between two sequential actions.

5.1.2 Control and Protection against AC Faults

Due to the complexity of the OWF integrated MMC MTDC system, different types of AC

faults may occur at different locations. Different types of AC faults and different fault locations have different impacts on the system fault characteristics [35]. Control and protection strategies against different faults vary according to different fault characteristics [35].

In an MMC MTDC system, the impact of an AC fault on the system is considered to be less significant than that of a DC fault [4], [7], [22] and the traditional control and protection against a common AC fault has been comprehensive [88]-[89]. It is generally considered that AC faults can be isolated by tripping AC circuit breakers. This is the case when the fault occurs within the protection range of the AC circuit breakers and the fault can be easily isolated by tripping the AC circuit breakers on both sides. However, this is not necessarily valid, since the fault may occur beyond the protection area of the AC circuit breakers [138]. In MMC MTDC systems, when a fault occurs at the MMC AC-side inside the converter station, which is beyond the protection area of the nearby AC circuit breakers, the fault isolation may require additional control and protection actions. This chapter investigates such a condition. The minimum time for detecting and locating an AC fault can be as fast as 2 ms [139]–[140]. There are several methods that are widely used for fault detection and location [141]–[143], e.g. overcurrent protection, distance protection, and current differential protection. However, for the fault isolation, since the fault arc has to be extinguished at current zero-crossing-point for the minimum impact and the AC current crosses zero-point at every half cycle, which is 10 ms for a 50 Hz power system, the fault isolation time is to be occurred at 10 ms [144]–[146] , However, considering the delay in the fault detection and isolation, and the delay in the operation of mechanical elements, faults are generally isolated in the range of 60-100 ms. The focus of this chapter is on the fault isolation strategy after the fault location and it is assumed that the fault has been detected and located. The fault

investigated is a permanent three-phase to ground fault, which occurs at different locations.

In Section 5.2, the fault occurring at the AC-side of MMC-1 is investigated. In Section 5.3, the fault occurring at the AC-side of MMC-2 is investigated. The corresponding control and protection strategy is proposed for each condition.

When an AC fault occurs at the MMC AC-side, if the control of the MMC is designed with a current limiter and the current limiter works normally, the fault current from the MMC AC-side can be limited. However, if the MMC applies V_{ac}-f control or the current limiter does not function as expected, there will be significant fault current flowing from the MMC AC-side. In addition to that, when the fault is a permanent AC fault, it would be expected to physically isolate the fault. It is generally achieved by blocking the faulted-side converter and tripping the AC circuit breaker at the other side, where an assumption has been made that the faulted-side converter can be blocked successfully. However, considering the practical operation of advanced MMCs, this assumption is not necessarily valid and Section 5.4 explores this issue of different conditions of blocking failure of the faulted-side MMC.

5.2 Control and Protection Against the Converter-Side AC Fault at the Power Regulated Terminal

T1, T3 and T4 are all transferring active power from/to the DC grid and are considered to be power regulated terminals. When a permanent fault occurs at the AC-side of one of these slave terminals, the fault should be physically isolated. In this section, the analysis is made for the fault occurring at T1, while the control and protection strategy proposed can be similarly applied for that which occurs at T3 or T4.

5.2.1 Fault Characteristics and Fault Isolation

When the fault occurs, the voltage at the faulted point will drop and the fault current will flow from the system AC-side and the MMC AC-side, which is illustrated in Figure 5-2.

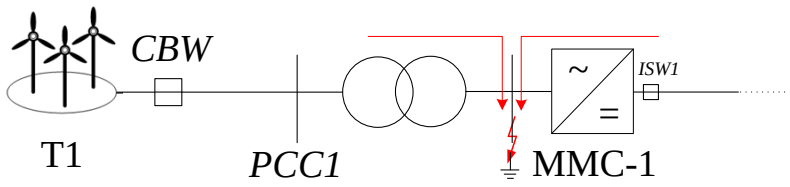


Figure 5-2 Three-phase to ground fault at the AC-side of MMC-1

At the system AC-side, the voltage drop at the faulted point will directly cause the terminal voltage of the OWF to deviate from the nominal value, which will lead to the oscillations of the output power of the OWF. At the MMC AC-side, the fault current flows into the faulted point from the DC-side through the MMC. Due to a permanent AC fault, if there is no effective control and protection applied, the fault will have an impact on the adjacent unfaulted terminals.

Hence, the fault needs to be speedily isolated. Firstly, the faulted-side MMC, MMC-1, will be swiftly blocked after detecting and locating the fault, leaving the fault current flowing only through the unilateral conductive diodes, which will finally prevent the DC current flowing to the MMC AC-side. Secondly, *CBW* will be tripped to isolate the faulted point from the AC system side and thus the OWF will not be further affected by the fault. The fault isolation by both blocking *MMC-1* and tripping *CBW* is illustrated in Figure 5-3.

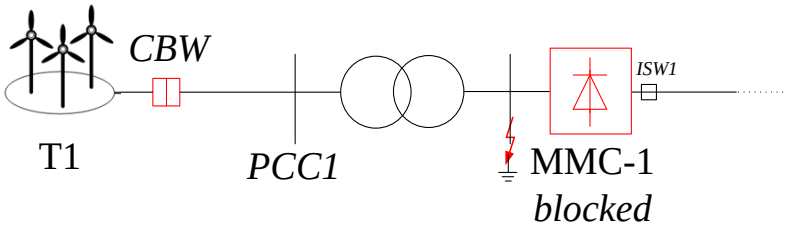


Figure 5-3 Fault isolation by blocking of MMC and tripping of AC circuit breaker

5.2.2 Faulted Section Isolation

After the fault isolation, the OWF terminal has lost the stable nominal voltage and the path for power transfer. Hence, the OWF will be blocked with the tripping of *CBW*. At the DC side, since T1 has been out of service, *ISW1* will be open when the current becomes sufficiently small. The objectives of opening *ISW1* are 1) to remove DC Cable 1 from the operation so as to avoid the power losses due to cable charging and discharging; 2) to physically isolate the fault by the mechanical switch to achieve the faulted section isolation. The faulted section isolation by opening *ISW1* is illustrated in Figure 5-4.

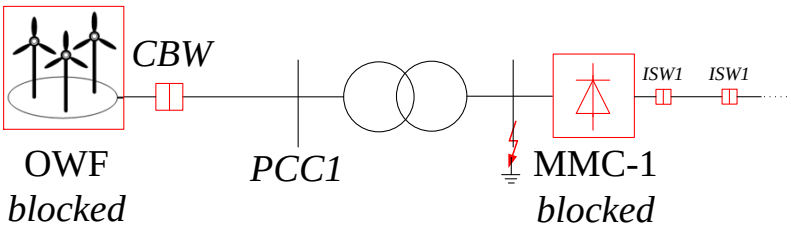


Figure 5-4 Faulted section isolation

If the fault is temporary, the faulted terminal can be resumed after clearing the fault. However, since the fault is permanent, the faulted terminal will not resume and the system will be reconfigured into 3-terminal MMC MTDC system.

5.2.3 Control and Protection Sequence

After the faulted section isolation, the faulted side is isolated from the DC grid. During the fault isolation and the faulted section isolation after the fault occurs, the unfaulted terminals are not significantly influenced: the DC voltage is maintained by MMC-2 and the active power is nominally transferred from MMC-3 and MMC-4. Therefore, the unfaulted terminals are normally operated without interruption and hence there is no need to conduct the system recovery of Phase 5 shown in Figure 5-1.

The complete control and protection sequence under the AC fault is depicted in Figure 5-5, the control action at each instant, t_n (n = 1,…,n) and the timing of t_n based on real-time simulation are presented in Table 5-1. The order of the control actions is the main focus of the proposed control and protection sequence, while the time delay between two sequential control actions is not the main focus.

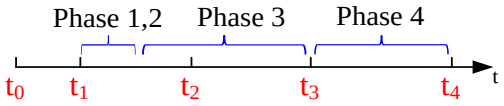


Figure 5-5 Control and protection sequence against AC fault at the AC-side of MMC-1

According to published literature and reports of industrial practice [22], [35], [55], [147], the IGBTs in an MMC can normally be blocked within 2-5 ms, the AC circuit breaker can be tripped within 60-100 ms and DC *ISW* can be opened when the current becomes sufficiently small. According to simulation studies, the fault current from the AC-side of MMC-1 increases over 1.2 p.u. within 8 ms, which is the assumed current threshold. Hence, it is assumed that MMC-1 is blocked when the current threshold is surpassed at 2.008 s, the tripping of AC circuit breaker is 80 ms after the fault and the DC *ISW* is opened at the current-

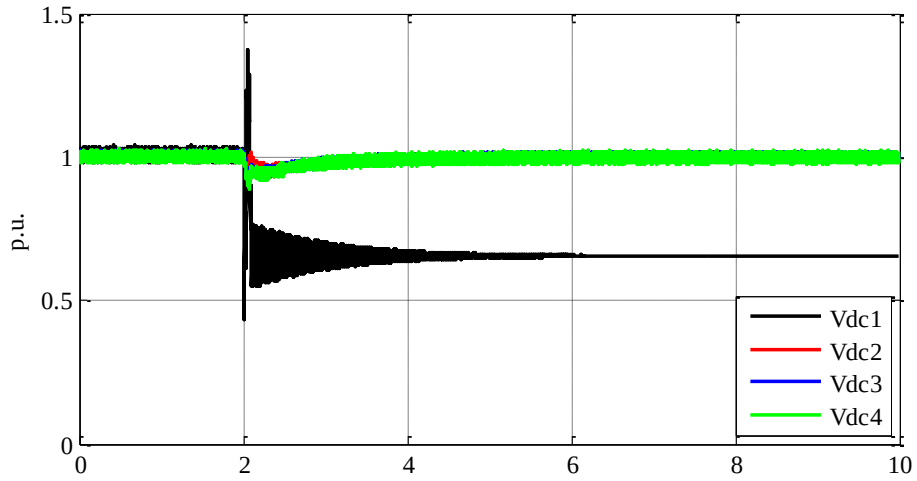
crossing-zero point.

Table 5-1 Description of the Operation and Timing of the Control and Protection Sequence in Figure 5-5

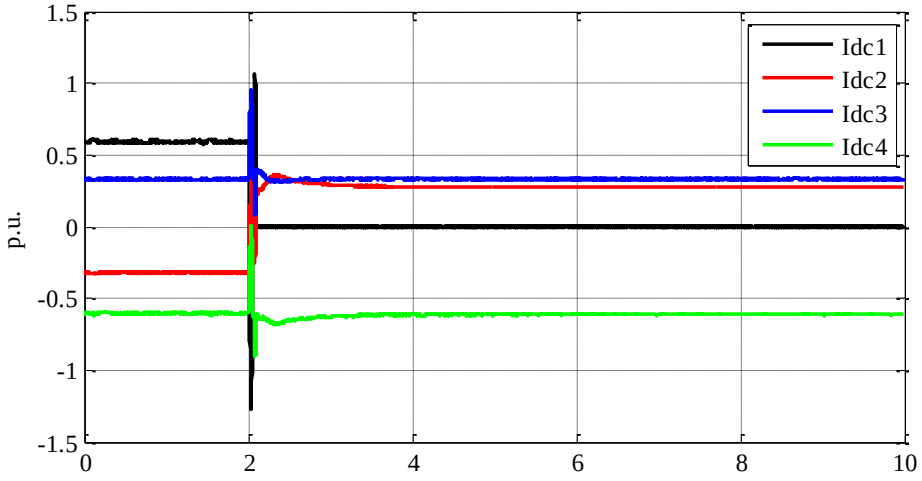
t_n	Time	Description	Comment
t_0	0 s	System under normal operation	
t_1	2 s	Apply the AC fault at the AC-side of MMC-1	
t_2	2.008 s	Block MMC-1	An MMC can be blocked as fast as 2-5 ms [35], [55], [147];
t_3	2.08 s	Trip *CBW* and block the OWF	An AC CB can generally be tripped within 60-100 ms [35], [55], [147];
t_4	2.44 s	Open DC ISW_1	A DC *ISW* can be opened when its current becomes sufficiently small.

5.2.4 Simulation Case Study

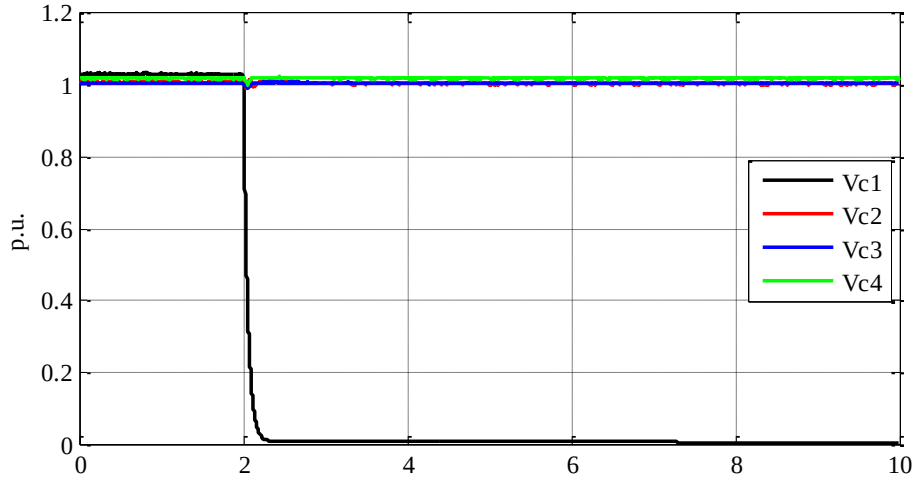
A three-phase to ground permanent fault is applied at 2 s at the AC-side of MMC-1. The system performance using the proposed control and protection sequence in Section 5.2.3 is demonstrated in Figure 5-6: (a) DC voltages of the MTDC; (b) DC currents of the MTDC; (c) MMC AC-side voltages in RMS value; (d) MMC AC-side currents in RMS value; (e) active power; (f) reactive power.



(a) Time (s)



(b) Time (s)



(c) Time (s)

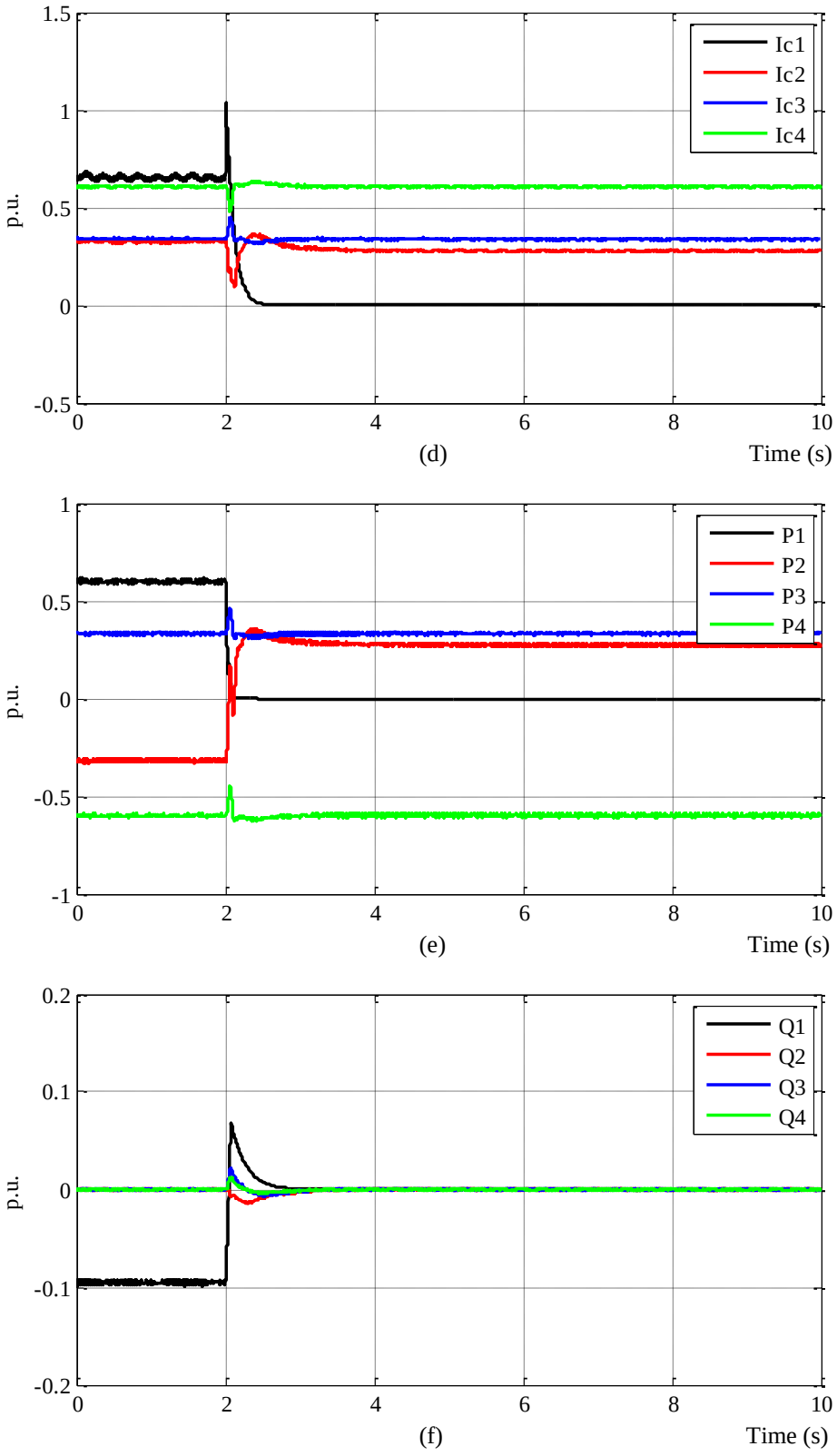


Figure 5-6 System performance under an AC fault at the AC-side of MMC-1 using the proposed control and protection sequence

Figure 5-6(a) demonstrates that the DC voltage at T1 oscillates after the fault occurs. The unfaulted-side DC voltages have a small drop and soon resume to the nominal value, which indicates that the fault is well isolated. Figure 5-6(b) shows that the DC currents oscillate when the fault occurs. The DC current at T1 reduces to zero when DC *ISW1* is opened. The loss of current is balanced by the control of MMC-2. The DC current transferred at T3 and T4 is maintained at the nominal value due to the effective fault isolation. The MMC AC-side current in Figure 5-6(d) and the active power in Figure 5-6(e) both have the similar performance to that of the DC current in Figure 5-6(b) where T2 balances the current/power loss of T1 and the current/power transferred at T3 and T4 is maintained at the nominal value. Since the fault is applied at the AC-side of MMC-1 and due to effective control and protection strategy, the MMC AC-side voltages at the unfaulted terminals are not significantly influenced as shown in Figure 5-6(c). Figure 5-6(f) demonstrates that the oscillations of the reactive power are small. In this case, the fault is effectively isolated using the proposed control and protection sequence and the unfaulted terminals is well protected and can continue operation.

5.3 Control and Protection against the Converter-Side AC Fault at the Master Terminal

Due to the fact that T2 is the master terminal which controls the DC voltage of the MTDC grid, the control and protection strategy against a fault at the AC-side of MMC-2 will be different to that against a fault at the other terminals.

5.3.1 Fault Characteristics and Fault Isolation

When a three-phase to ground fault occurs at the AC side of MMC-2, fault current will flow

from both the MMC-AC side and the AC system side as illustrated in Figure 5-7.

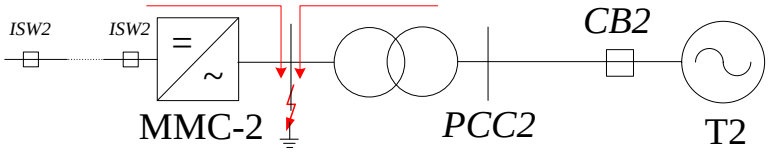


Figure 5-7 AC fault occurs at the AC-side of MMC-2

Meanwhile, the voltage at the faulted point will drop when the earth fault occurs. Due to the voltage drop at the AC-side of MMC-2, the voltage at *PCC2* and at the DC-side of MMC-2 will both decrease. Since the *dq* decoupled control requires the stable nominal voltage at the PCC, the voltage fall at *PCC2* will significantly affect the performance of MMC-2. The voltage fall at the DC-side of MMC-2 will lead to the voltage drop of the MTDC grid, since T2 is the master terminal of the MTDC grid to maintain the DC voltage. The whole MTDC system may collapse if no effective control and protection operation is applied after the fault occurs, particularly under a permanent fault.

Therefore, the fault must be speedily isolated by blocking MMC-2 and tripping *CB2*, which is illustrated in Figure 5-8.

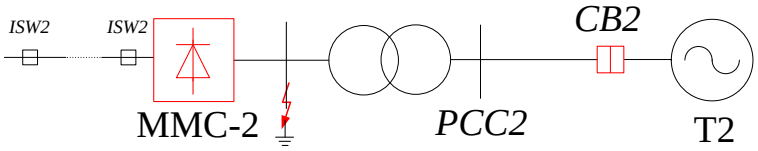


Figure 5-8 Control and protection strategy for the fault isolation

MMC-2 will lose control on the DC voltage after being blocked and thus the MTDC grid will lose stable DC voltage. Under this condition when the DC voltage is out of control, the other 3 terminals must stop transferring power into the DC grid. Therefore, the MMCs at the

unfaulted terminals need to be swiftly blocked after the blocking of MMC-2. Since the voltage at *PCC1* will not be stabilised after blocking MMC-1, the OWF should also be blocked. Considering the fact that the OWF is a weak AC system, it would be better to isolate the OWF during the fault by tripping *CBW* and to re-integrate the OWF after the faulted section isolation. The current system status is illustrated in Figure 5-9.

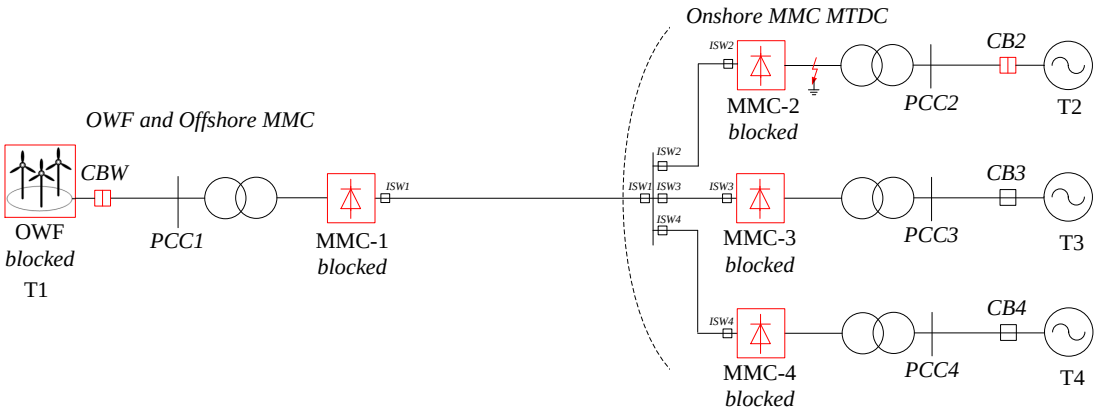


Figure 5-9 System status after the fault isolation at the master terminal

5.3.2 Faulted Section Isolation

The faulted section is isolated by opening *ISW2* when the current becomes sufficiently small. The system state after the faulted section isolation is depicted in Figure 5-10.

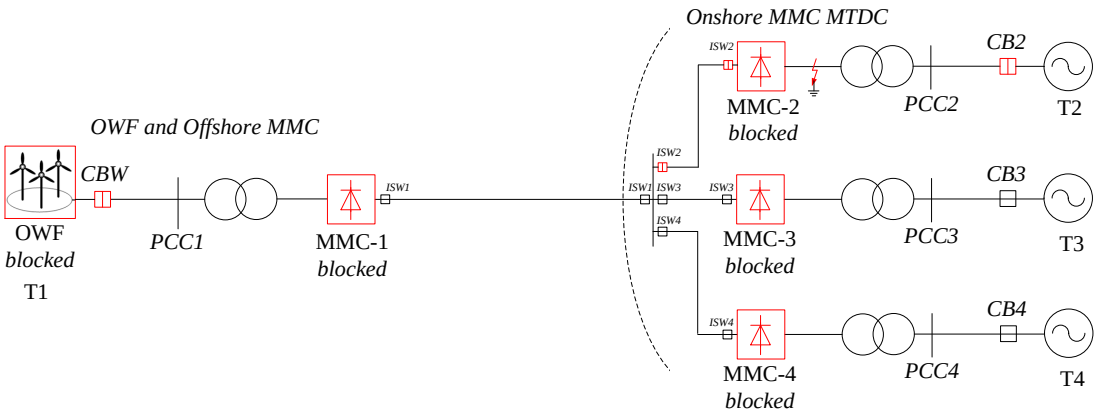


Figure 5-10 System status after the faulted section isolation at the master terminal

After the faulted section isolation, both MMC-2 and the other 3 MMCs are blocked and the DC voltage becomes out of control. Due to a permanent earth fault, T2 will not resume. Hence, there are 2 options at this stage:

- The unfaulted terminals do not resume operation;
- If the unfaulted terminals are scheduled to resume, one of them needs to take over the control of the DC voltage and the other terminals will then resume after the DC voltage being stabilised.

5.3.3 Control and Protection Sequence

The second condition is considered in this chapter with a comprehensive control and protection sequence proposed. In practical operation, it is preferable that the control of a converter is kept at a fixed control mode rather than switch to another control mode during operation. However, under some special conditions such as after the faulted section isolation, all converters are at standby mode and the master converter cannot resume due to a permanent fault, as flexible VSC-based MMC technique, a back-up control mode should be arranged for changing the control mode and resuming the unfaulted terminals. For this case, MMC-4 is selected to take over the control of the DC voltage and performs as the master converter. A comprehensive control and protection sequence is proposed in Figure 5-11 in which the control action at each instant and the delay between two sequential actions are presented in Table 5-2.

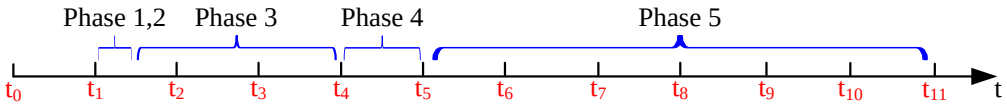


Figure 5-11 Comprehensive control and protection sequence under AC fault at MMC-2 AC-side

Table 5-2 Description of the Control and Protection Sequence in Figure 5-11

t_n	Time	Description	Comment
t_0	0 s	System under normal operation	
t_1	2 s	Apply the AC fault at the AC-side of MMC-2	
t_2	2.010 s	Block MMC-2	An MMC can be blocked as fast as 2-5 ms. Here a delay of blocking the unfaulted-side MMC is considered;
t_3	2.015 s	Block the other 3 MMCs	
t_4	2.08 s	Trip *CB2* and *CBW*, block the OWF	An AC CB can generally be tripped within 60-100 ms ;
t_5	2.14 s	Open *ISW2*	A DC *ISW* can be opened when its current becomes sufficiently small.
t_6	6 s	Change MMC-4 to V_{dc} control	A delay of 2 s is set between two sequential control actions. This delay can be shortened as long as the system reaches a steady condition after the former control action.
t_7	8 s	Deblock MMC-4	
t_8	10 s	Deblock MMC-3	
t_9	12 s	Deblock MMC-1	
t_{10}	17 s	Reclose *CBW*	The re-integration of the OWF needs a stable AC voltage at *PCC1*. Hence, a long delay of 5 s is chosen.
t_{11}	18 s	Deblock the OWF	

According to simulation studies, the fault current from the AC-side of MMC-2 increases over 1.2 p.u. within 10 ms, which is the assumed current threshold. Hence, MMC-2 will be blocked at 2.010 s, while the other 3 MMCs are assumed to be blocked with 5 ms delay. The comprehensive control and protection sequence shown in Figure 5-11 consists of fault isolation, faulted section isolation and recovery of the unfaulted terminals. The detailed control actions and the delay between two sequential actions are fully considered after the

fault location, and the change of control mode of MMC-4 is included in the recovery of the unfaulted terminals. The system state after the recovery of the unfaulted terminals is illustrated in Figure 5-12.

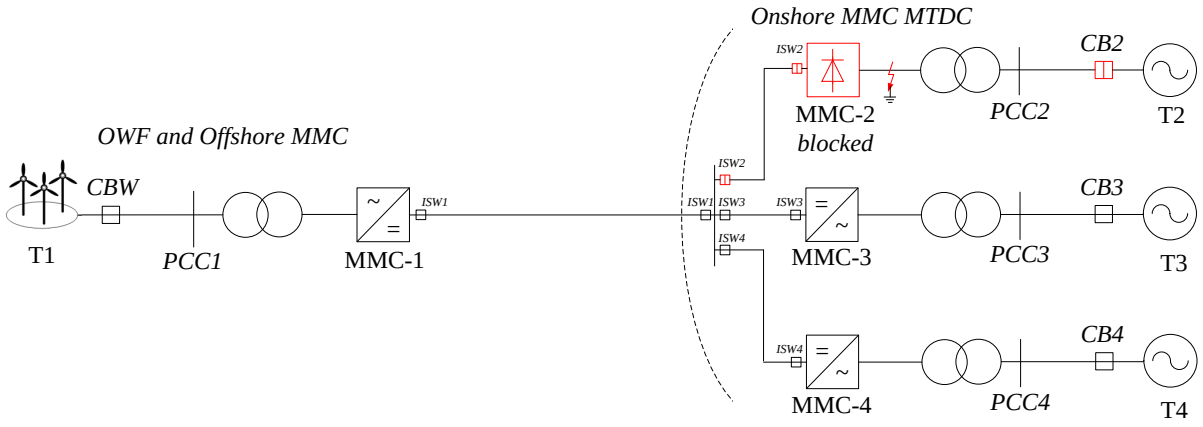
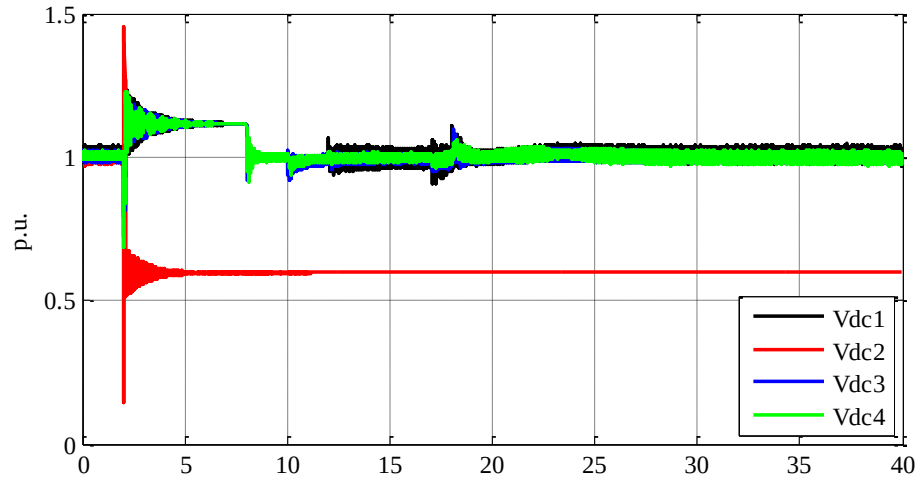


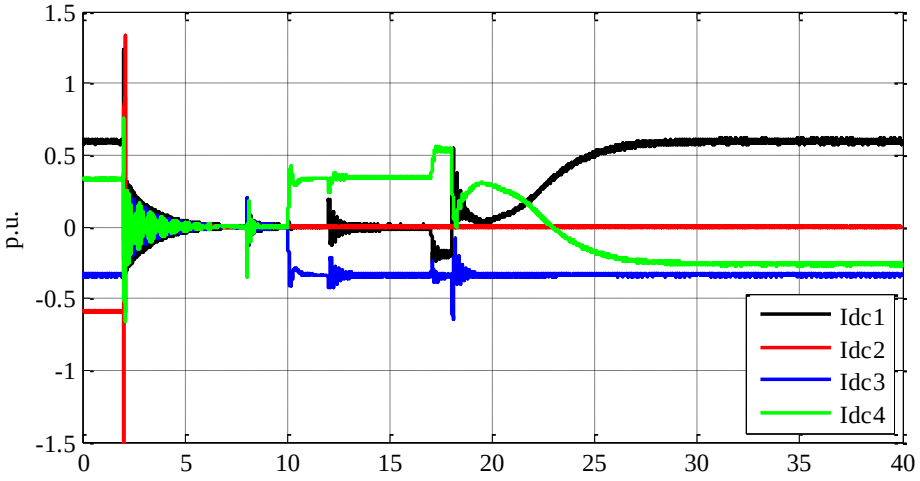
Figure 5-12 System state after the recovery of the unfaulted terminals

5.3.4 Simulation Case Study

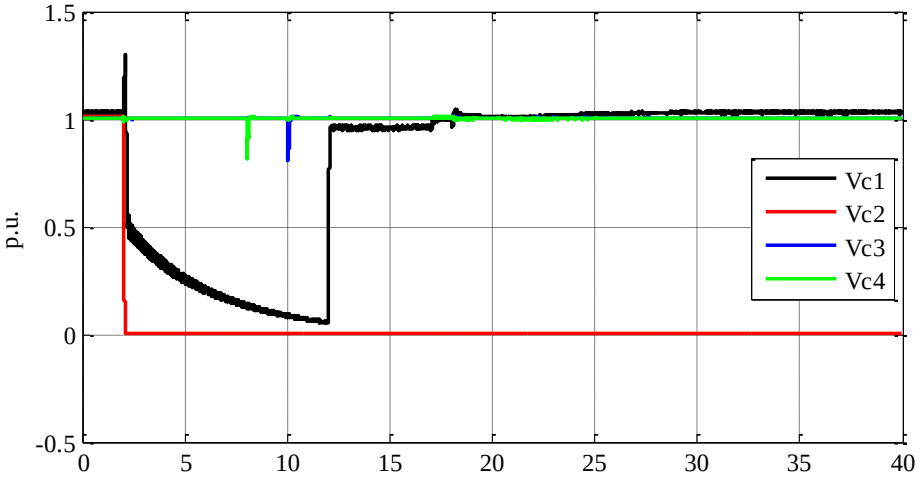
The permanent fault at the AC-side of the master converter is applied at 2 s, the system performance using the proposed control and protection sequence in Section 5.3.3 is demonstrated in Figure 5-13: (a) DC voltages of the MTDC; (b) DC currents of the MTDC; (c) MMC AC-side voltages in RMS value; (d) MMC AC-side currents in RMS value; (e) active power; (f) reactive power.



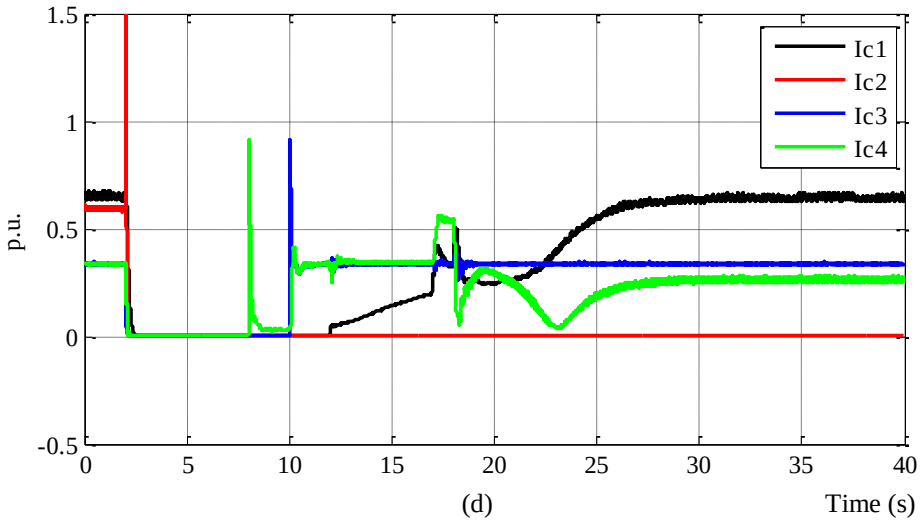
(a) Time (s)

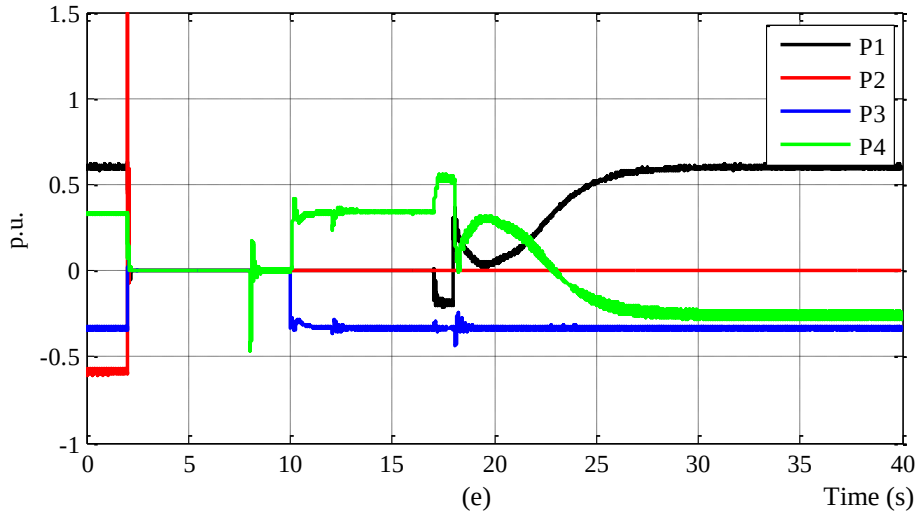


(b) Time (s)



(c) Time (s)





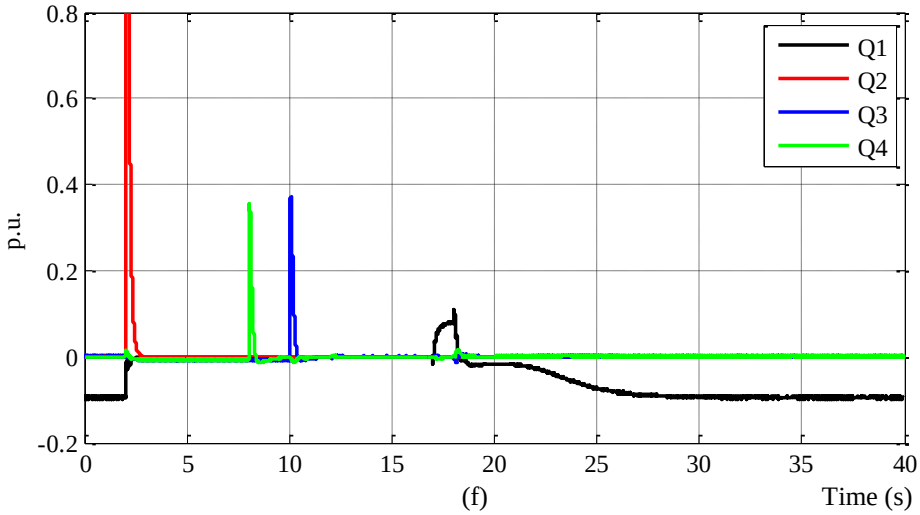


Figure 5-13 System performance under an AC fault at the AC-side of MMC-2 using the proposed control and protection sequence

Control and protection operation is conducted swiftly after the fault occurs to isolate the fault and *ISW2* is opened when its current decays to zero to isolate the faulted section. Figure 5-13(a) demonstrates that due to effective isolation of the faulted section, the DC voltage at T2 decreases to around 0.73 p.u. after oscillations and the DC voltages at the unfaulted terminals are maintained at around 1.1 p.u. after oscillations. When MMC-4 is deblocked at 8 s after its control mode being changed to DC voltage control, the DC voltage resumes to the nominal value and is well stabilised during the recovery period. Figure 5-13(b) shows that the DC currents gradually decay to zero instead of injecting into the faulted point, which indicates the fault has been completely isolated due to effective control and protection. After the re-establishment of the DC voltage by T4, the DC currents at the unfaulted terminals smoothly resume to the normal operating condition. The performance shown in Figure 5-13(d) and Figure 5-13(e) is similar to that of Figure 5-13(b). During the whole process, the MMC AC-side currents and the active power are both under the nominal value most of the time, except that after the fault occurs before the control and protection action, the current at MMC-2 AC-side has overcurrent and the active power at T2 is over the nominal value. After the faulted section isolation, the MMC AC-side current and the active power at the unfaulted terminals resume to the normal operating condition at the system recovery stage. Figure 5-13(c) demonstrates that due to effective fault isolation, the voltages at the AC-side of MMC-3 and MMC-4 are maintained at the nominal values almost without decrease. MMC-1 AC-side voltage reduces to a level approaching 0 since the OWF is isolated after the fault occurs and the voltage resumes to the nominal value when the OWF is re-integrated into the system. Figure 5-13(f) shows that the reactive power oscillations are not significant. The simulation results prove the feasibility and effectiveness of the proposed control and protection sequence.

5.4 Control and Protection Against Converter-Side AC Fault with the Faulted-Side MMC Blocking Failure

Previous analysis and proposed control and protection sequence in Section 5.2 and Section 5.3 were established based on the assumption that the faulted-side MMC was blocked successfully after the fault occurred. However, this assumption is not necessarily valid, especially for the MMC technique [138]. Since there are tens to hundreds of SMs on each converter arm and the operation of the SM is independent of each other, different conditions of blocking failure could emerge following an AC or DC fault. Some conditions of blocking failure may render the proposed control and protection ineffective, that is, the fault isolation is not fully achieved. In this section, the proposed control and protection in the previous section is named as "basic control and protection".

Different conditions of blocking failure are categorised into non-emergency condition and emergency condition, according to the system performance with basic control and protection after a fault occurs with different blocking failure of the faulted-side MMC. The non-emergency condition is that the basic control and protection can still effectively isolate the fault under the blocking failure of the MMC. However, although the basic control and protection is sufficient in the non-emergency conditions, some potential risks may emerge. The emergency condition is that the basic control and protection becomes invalid and cannot fully isolate the fault under the blocking failure of the MMC. Under the emergency condition, a special control and protection scheme is proposed to isolate the fault.

An MMC could have different conditions of blocking failure: a) whole converter blocking failure; b) one converter arm completely fails to be blocked; c) one converter arm partly fails

to be blocked such as one/several SMs fails to be blocked; d) other conditions. In the first 3 conditions, a) is considered to be rare, but it may occur at the communication outage of control signals where the whole converter could be completely out of control and fails to be blocked. c) is considered to be the most common one, since there are tens to hundreds of SMs in one MMC and one or more of them may fail to be blocked.

The following sub-sections will investigate these 3 conditions. The research emphasis is put on determining whether each condition is emergency condition or non-emergency condition according to the analysis and real-time simulations, and proposing an effective special control and protection scheme for the emergency condition. The fault is applied at the AC-side of MMC-1, hence the blocking failure is assumed to occur on MMC-1.

5.4.1 Whole MMC Blocking Failure

For a permanent earth fault occurring at the AC-side of MMC-1, the basic control and protection strategy is to block MMC-1 and the OWF, trip *CBW* and open *ISW1*, according to previous analysis. When MMC-1 completely fails to be blocked, the system state at T1 after the fault is illustrated in Figure 5-14.

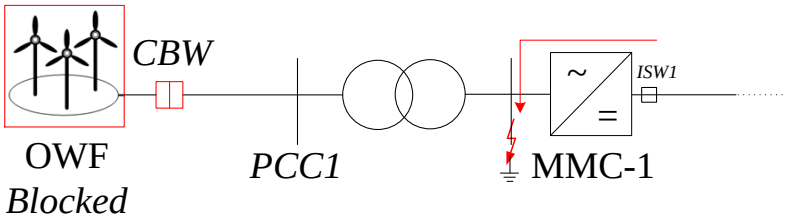


Figure 5-14 System state at T1 after the fault under MMC-1 completely blocking failure

Since MMC-1 has a complete blocking failure, only the AC system side is isolated after tripping *CBW*, while the DC side is not isolated from the faulted point. Therefore, the current

at the DC-side will flow into the faulted point through MMC-1.

The performance of the AC-side RMS current of MMC-1 under the permanent fault at 2 s with MMC-1 complete blocking failure is demonstrated below in Figure 5-15: (a) MMC-1 AC-side current in RMS value; (b) zoomed proportion of (a).

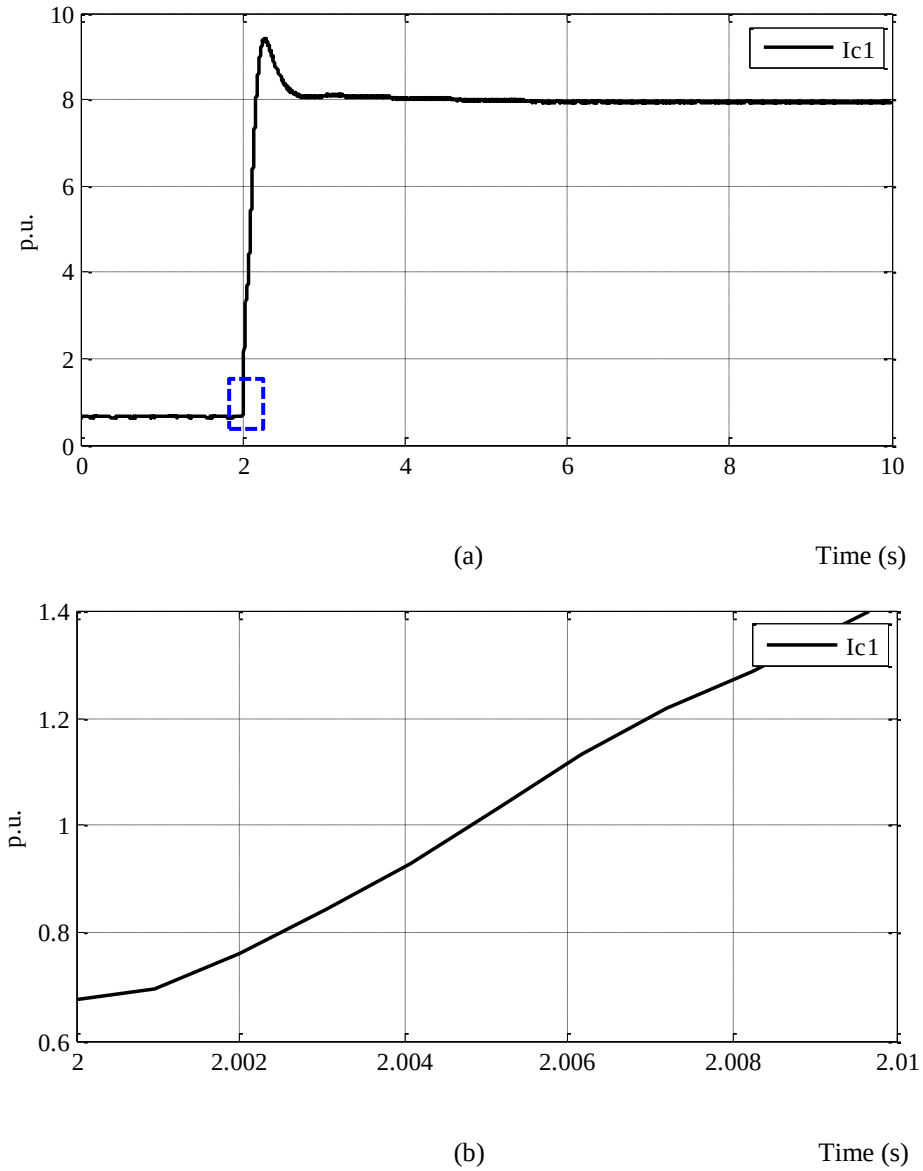


Figure 5-15 Performance of the AC-side RMS current of MMC-1 under MMC-1 AC-side fault with MMC-1 complete blocking failure using the basic control and protection sequence

Figure 5-15(a) demonstrates that the current at MMC-1 AC-side increases continuously after the fault occurring at 2 s due to the complete blocking failure of MMC-1. The fault current from MMC-1 AC-side finally increases to around 8 p.u.. It indicates that the fault isolation is not achieved. In addition, the IGBTs in MMC-1 may be damaged under such a large overcurrent when MMC-1 experiences complete blocking failure. A calculation of the fault current is presented in Appendix D for the justification of the simulation result.

Based on the analysis and simulation results, it can be seen that the fault is not isolated using the basic control and protection strategy. Therefore, complete blocking failure of MMC-1 is considered to be the emergency condition, necessitating special control and protection. In order to protect the IGBTs, the MMCs at the unfaulted terminals will be blocked once the failure of the fault isolation is identified. Here the MMCs at the other 3 terminals are blocked with 5 ms delay when the fault current at any terminal is detected to be over 1.2 p.u..

Figure 5-15(b) shows that the fault current at the AC-side of MMC-1 increases over 1.2 p.u. within 8 ms. Hence, the MMCs at the unfaulted terminals are assumed to be blocked with 5 ms delay at 2.013 s. However, due to the unilateral conductive characteristics of diodes, the current at the AC side can still feed into the DC grid. Therefore, the CBs at the unfaulted terminals need to be tripped to achieve the fault isolation. The current system status with the special control and protection strategy is illustrated in Figure 5-16.

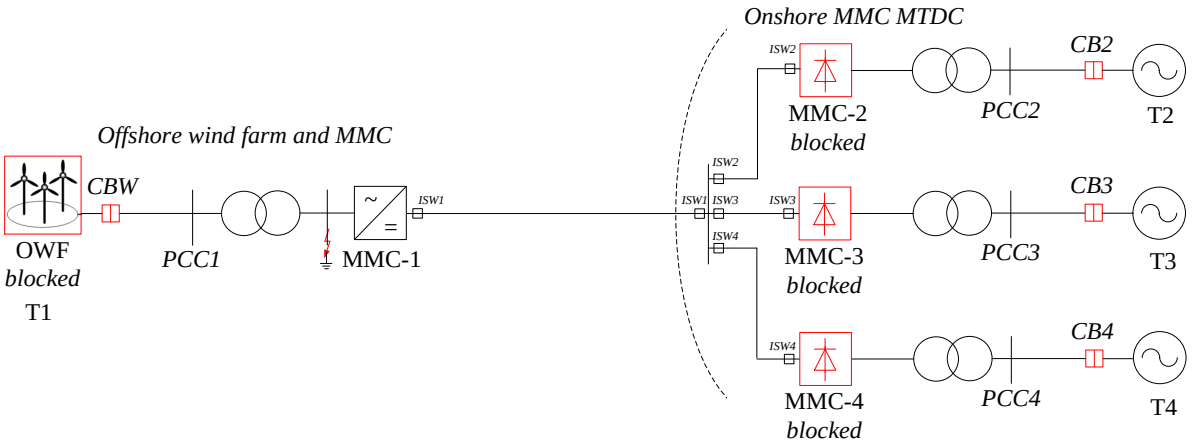


Figure 5-16 System status with special control and protection to achieve the fault isolation

Since all the CBs have been tripped, there is no power source feeding into the DC grid and the DC currents will gradually decay to 0. *ISW1* will be opened when the DC current at T1 becomes sufficiently small to achieve the faulted section isolation. In the simulation, *ISW1* is opened at current-crossing-zero point. The current system state is illustrated in Figure 5-17.

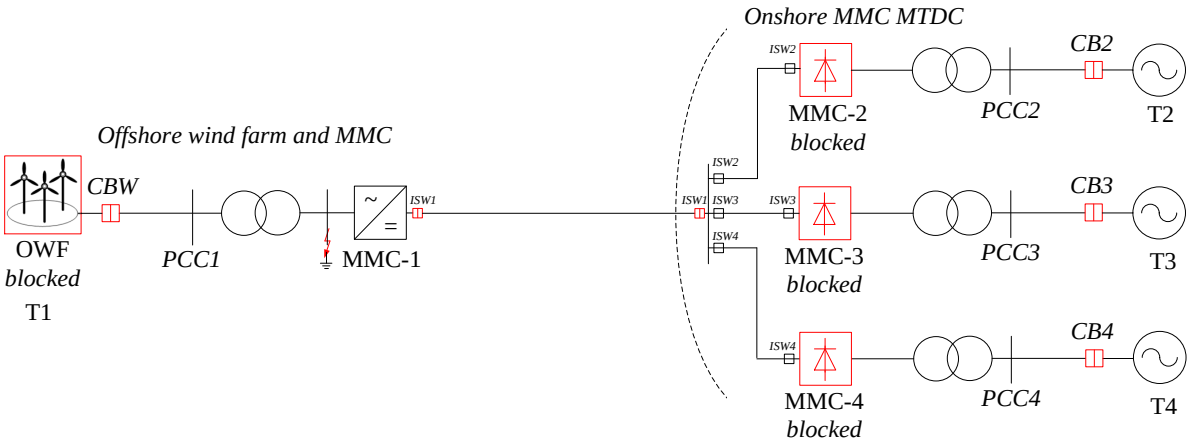


Figure 5-17 System state with special control and protection to achieve the faulted section isolation

The special control and protection sequence for the fault isolation and the faulted section isolation is illustrated in Figure 5-18. Table 5-3 presents the control action at each instant and the delay between two sequential control actions.

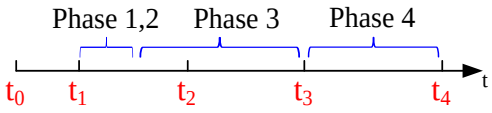
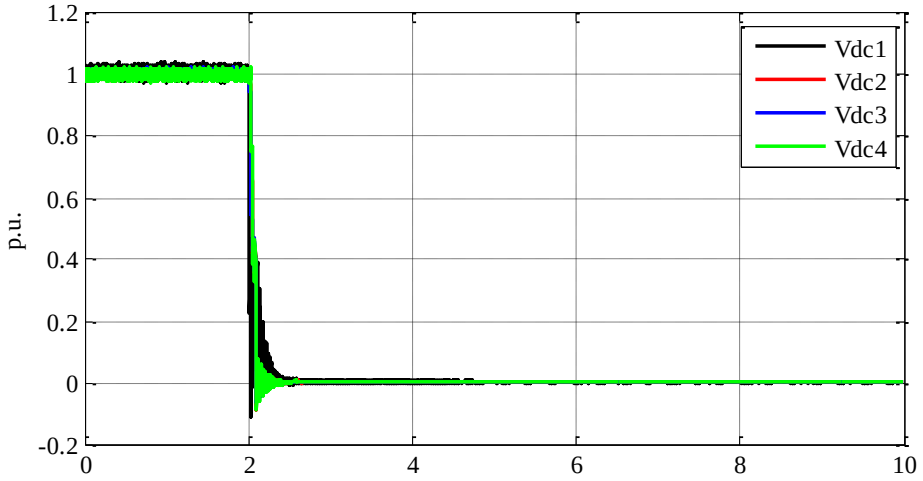


Figure 5-18 Special control and protection sequence for the fault isolation and faulted section isolation under AC fault at MMC-1 AC-side with complete blocking failure of MMC-1

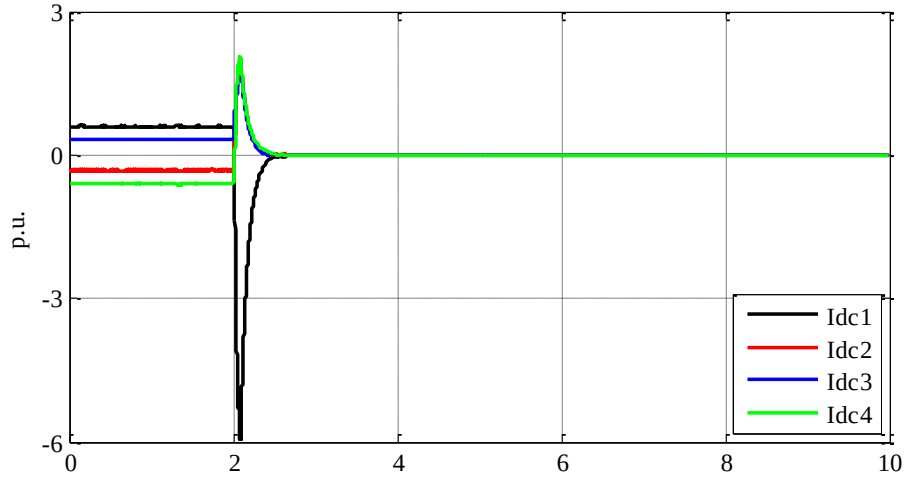
Table 5-3 Description of the Control and Protection Sequence in Figure 5-18

t_n	Time	Description	Comment
t_0	0 s	System under normal operation	
t_1	2 s	Apply the AC fault at the AC-side of MMC-1	
t_2	2.013 s	Block MMC-2, MMC-3 and MMC-4	An MMC can be blocked as fast as 2-5 ms. Here a delay of blocking the unfaulted-side MMC is considered;
t_3	2.08 s	Trip *CBW*, block the OWF, trip *CB2*, *CB3*, *CB4*	An AC CB can generally be tripped within 60-100 ms;
t_4	2.124 s	Open *ISW1*	A DC *ISW* can be opened when its current becomes sufficiently small.

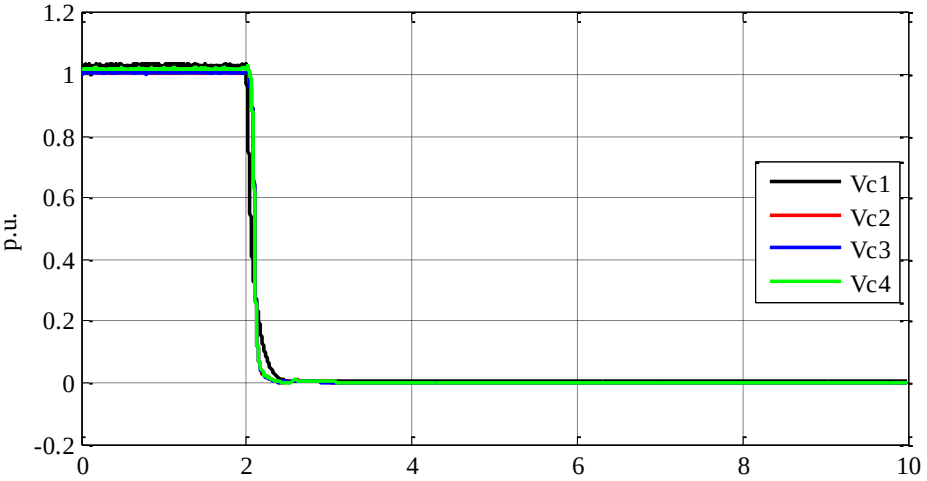
Using the proposed special control and protection sequence, the system performance is demonstrated in Figure 5-19: (a) DC voltages of the MTDC; (b) DC currents of the MTDC; (c) MMC AC-side voltages in RMS value; (d) MMC AC-side currents in RMS value; (e) active power; (f) reactive power.



(a) Time (s)



(b) Time (s)



(c) Time (s)

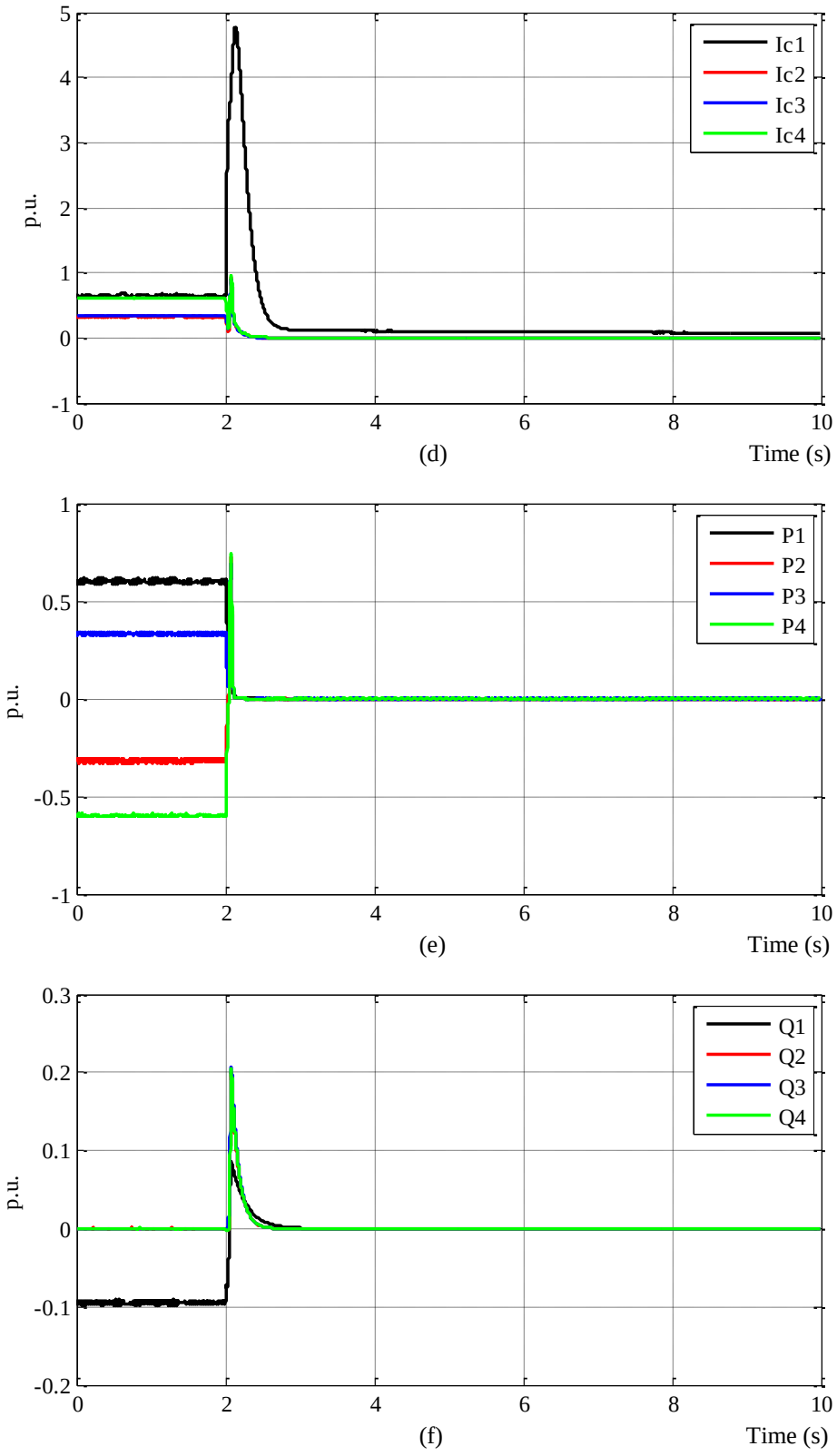


Figure 5-19 System performance under an MMC-1 AC-side fault with complete blocking failure of MMC-1 using the proposed special control and protection

Figure 5-19(a) demonstrates that due to effective control and protection, the DC voltages decrease to 0 and no significant oscillations emerge at T1. Figure 5-19(b) shows that the DC currents start to decrease when the AC circuit breakers are tripped at 2.08 s and finally decay to 0. However, the DC overcurrent at T1 after the fault is large and increases to around 6 p.u., which is considered as a potential risk. Figure 5-19(c) shows that the MMC AC-side voltages decrease to 0 after the control and protection action. Figure 5-19(d) demonstrates that MMC-1 AC-side current starts to decrease after *ISW1* is open and finally decays to 0. Although the overcurrent at MMC-1 AC-side is still large using the special control and protection, the current surge is smaller than that in Figure 5-15 using the basic control and protection. Figure 5-19(e) shows that the active power at each terminal decreases to 0 with almost no oscillations. Figure 5-19(f) shows that the reactive power at each terminal increases after the fault occurs and decreases to 0 after the control and protection action.

The analysis and simulation results prove that the special control and protection strategy can effectively isolate the fault and faulted section. However, potential risks of overcurrent at the AC-side and DC-side of MMC-1 with complete blocking failure still exist.

After the faulted section isolation, the unfaulted terminals can resume operation. The emphasis of this section is put on the special control and protection strategy for the fault isolation and the faulted section isolation under the emergency condition. The recovery of the unfaulted terminals after the faulted section isolation is not discussed in this section. In the next chapter, control and protection against DC faults will be investigated and particular attention will be paid on the system recovery after the faulted section isolation. The proposed control and protection strategy and sequence at the system recovery stage can also be applied for the case in this section, since both system states after the faulted section isolation is

similar.

5.4.2 One Converter Arm Complete Blocking Failure

In this section, one arm of MMC-1 has complete blocking failure after the fault occurs is investigated. This condition, in comparison with whole blocking failure of MMC-1, is less severe. When one arm of MMC-1 has complete blocking failure, taking the upper arm of Phase A as an example, the current system status at T1 is illustrated in Figure 5-20.

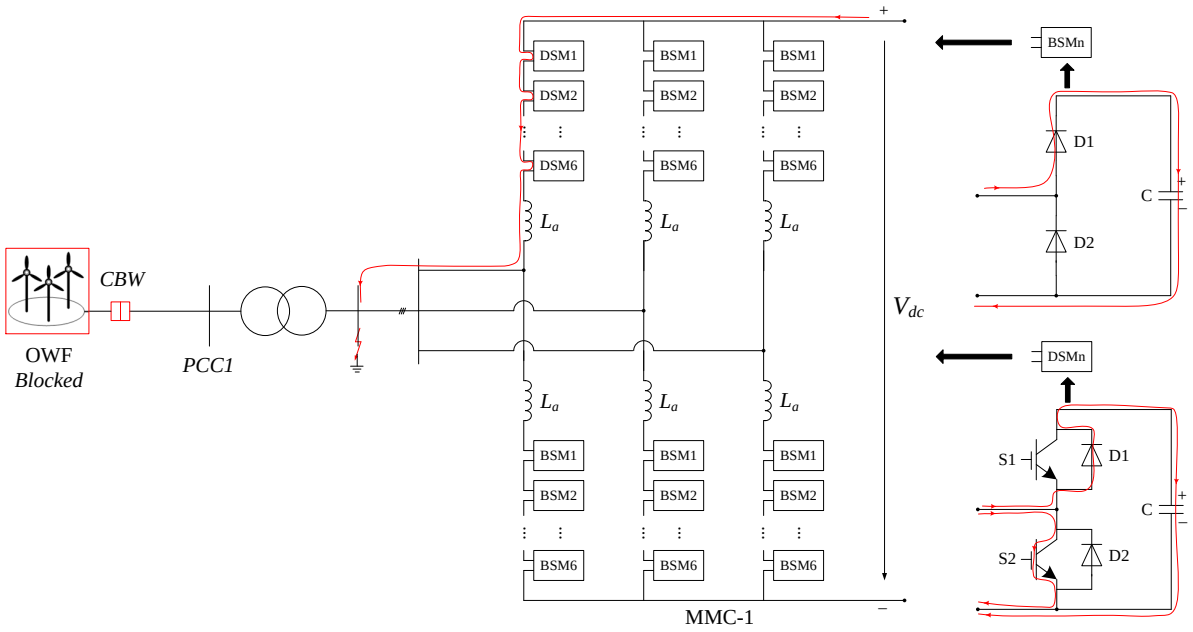


Figure 5-20 System status at T1 with one arm complete blocking failure of MMC-1

In Figure 5-20, BSM*n* (*n* = 1,…,6) denotes the SM that is blocked successfully, DSM*n* (*n* = 1,…,6) denotes the SM that has blocking failure or is at deblocking state.

For those arms that are blocked successfully, the SM capacitors do not have any discharging path and can only be charged when the arm current flows through diode D1 and then into the faulted point. The arm currents gradually decrease with the SM capacitors being charged and they will decrease to zero when the voltage sum of the SM capacitors on one arm equals to

the voltage of DC positive-pole and thus stop flowing into the faulted point. Since the upper arm of Phase A has complete blocking failure, the SM capacitors on this arm have both paths of being charged and discharged. The current from the DC-side can flow into the faulted point through either diode D1 or IGBT S2 and cannot be prevented. The performance of the AC-side RMS current of MMC-1 under the permanent fault at 2 s with one converter arm complete blocking failure of MMC-1 is demonstrated below in Figure 5-21.

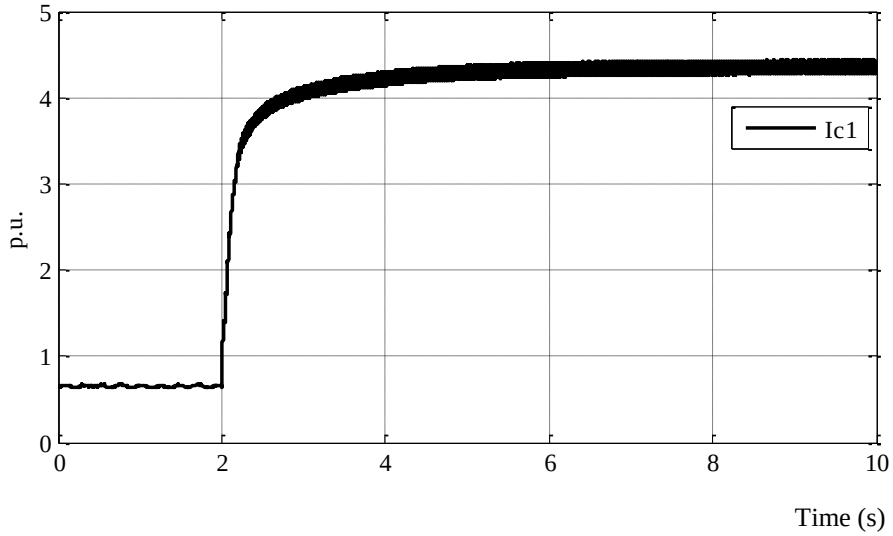


Figure 5-21 Performance of the AC-side RMS current of MMC-1 under the fault with MMC-1 one arm complete blocking failure using the basic control and protection sequence

The current at MMC-1 AC-side continuously increases to around 4.3 p.u. after the fault occurs. It indicates that the blocking failure on the upper arm of Phase A leads to the failure of the fault isolation. Since the blocking failure in this case occurs only on one converter arm, the condition is less severe than that of the blocking failure of the whole MMC.

According to the analysis and simulation results, it can be seen that the fault is not successfully isolated using the basic control and protection. Hence, it is necessary to apply the special control and protection strategy proposed in Section 5.4.1 to achieve the fault isolation

and faulted section isolation.

5.4.3 One Converter Arm Partly Blocking Failure

In this section, one arm of MMC-1 that has partly blocking failure is investigated. In comparison with the previous 2 conditions of blocking failure, the occurrence of this condition has a higher possibility. This is because each MMC has numerous SMs and one or some of them may experience blocking failure. In order to facilitate analysis, this condition is divided into 3 sub-conditions in which blocking failure only occurs on one arm of MMC-1: 1) All SMs but one blocking failure; 2) Half SMs blocking failure; 3) One SM blocking failure.

5.4.3.1 All SMs but one blocking failure

When the blocking failure occurs on one arm of MMC-1 in which only one SM is blocked successfully, the converter status is illustrated in Figure 5-22.

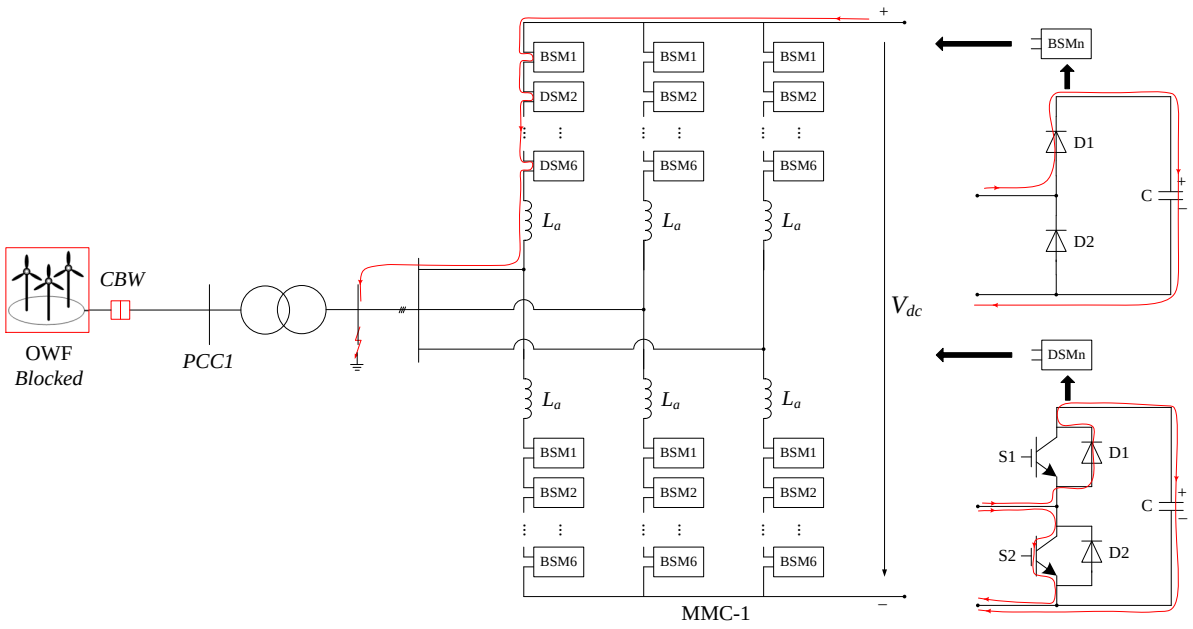
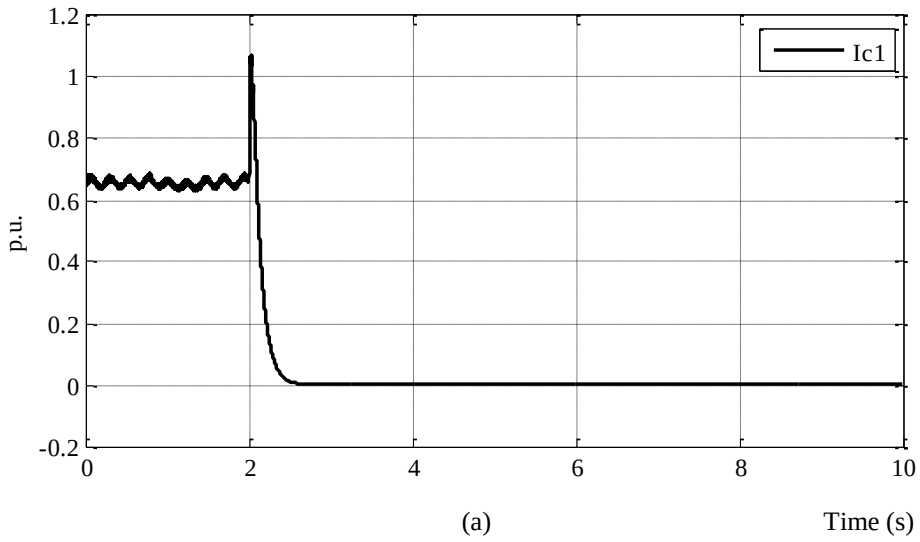


Figure 5-22 System status at T1 with one arm partly blocking failure of MMC-1 in which only 1 SM is blocked successfully

For the SM that is blocked successfully, its capacitor is charged when the arm current flows from the DC-side into the MMC AC-side and is bypassed when the arm current flows in the reversed direction. Hence, the capacitor has no discharging path and can only be charged, which is the operating Mode 3 of a SM as explained in Figure 2-6 in Section 2.3.2. The capacitor voltage increases gradually and will be finally charged to a value which equals to the voltage difference between the DC positive-pole and MMC-1 AC-side. The arm current gradually decreases and will finally decays to zero. Hence, the fault isolation is realised thanks to the successfully blocked SM. Nevertheless, a potential risk is that the blocked SM capacitor is overcharged and has an overvoltage. Since an earth fault occurs at MMC-1 AC-side, for the sake of simplicity of analysis, the voltage at MMC-1 AC-side can be assumed to be 0. Thus, the capacitor voltage of the only one SM which is blocked successfully will be charged a value close to the voltage of the DC positive-pole. Taking the upper arm of Phase A as an example of having blocking failure in which only one SM is blocked successfully, the system performance with basic control and protection is demonstrated in Figure 5-23: (a) MMC-1 AC-side current in RMS value; (b) DC voltages of the MTDC; (c) DC currents of the MTDC; (d) SM capacitor voltages of the upper arm of Phase A.



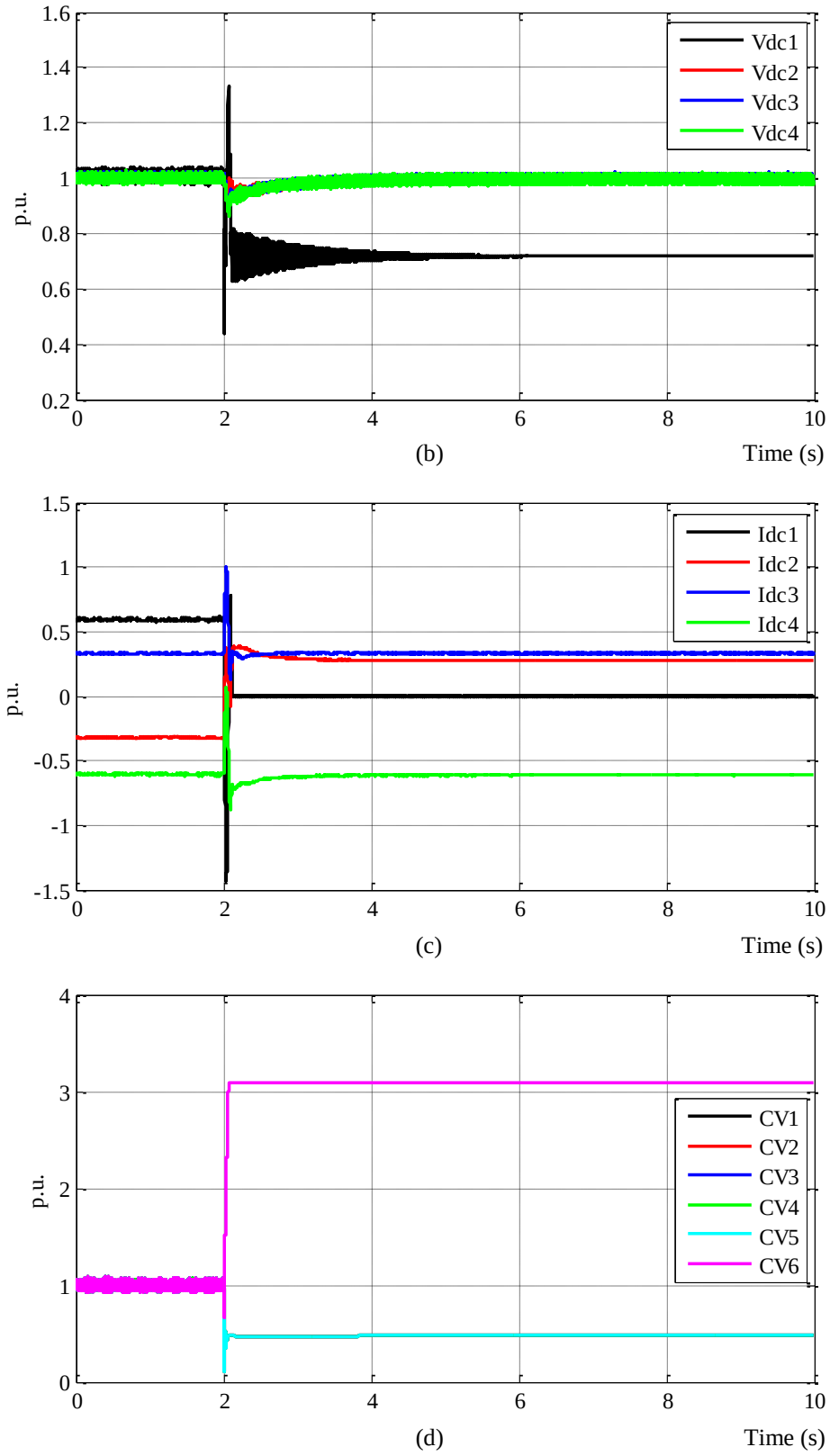


Figure 5-23 System performance under an MMC-1 AC-side fault with one arm of MMC-1 partly blocking failure (1 SM blocked successfully) using the basic control and protection

Figure 5-23(a) demonstrates that a small current surge emerges at MMC-1 AC-side after the fault occurs and the current gradually decays to 0 after the basic control and protection operation. It indicates that the basic control and protection has prevented the MMC-1 DC-side current feeding into the faulted point and the fault isolation has been achieved. Figure 5-23(b) shows that the DC voltages at the unfaulted terminals return to the nominal value soon after a small voltage drop following the fault. The DC voltage at T1 has a voltage spike after the fault and then gradually decreases to around 0.75 p.u. with oscillations since one arm of MMC-1 has partly blocking failure. In Figure 5-23(c), small current surges can be observed following the fault, while the DC currents at the unfaulted terminals do not further inject into T1. The DC currents at T3 and T4 return to their nominal values, the DC current at T1 decreases to 0 after the control and protection action and the DC current at T2 balances the loss of the current from T1. Figure 5-23(d) shows that the capacitor voltage of the SM, which is the only one blocked successfully on the upper arm of Phase A, is charged to over 3 p.u., which is close to the voltage of the DC positive-pole. Although the fault is isolated thanks to the SM which is successfully blocked, large overvoltage of the SM capacitor is a potential risk.

Since the capacitors of the successfully blocked SMs can only be charged and have no discharging path, the relationship between the capacitor voltage of these SMs and the MMC DC-side voltage can be derived as follows:

$$V_{BLK,SM} \geq \frac{V_{dcp}}{n} \tag{5.1}$$

where $V_{BLK,SM}$ is the voltage of one of the successfully blocked SMs, V_{dcp} is the voltage of the DC positive-pole, n is the number of successfully blocked SMs.

The nominal voltage of a SM under steady-state condition is $\frac{V_{dc}}{n}=\frac{V_{dcp}}{n/2}$. Therefore, the potential risk will emerge if the number of successfully blocked SMs is less than half of the SMs on one arm. Since the DC voltage at T1 will oscillate after the fault occurs leading to a voltage spike which may be larger than the nominal voltage at the DC positive-pole, there may still be small overvoltage on the successfully blocked SMs when half of the SMs are blocked successfully. The possibility of the emerging overvoltage will reduce with the increase of the number of successfully blocked SMs.

According to the analysis and simulation results, the condition that the blocking failure occurs on one converter arm in which only one SM is successfully blocked is non-emergency condition. The basic control and protection can achieve the fault isolation and it is not necessary to utilize the special control and protection. However, the successfully blocked SM has a potential risk of being overcharged.

5.4.3.2 Half converter arm blocking failure

When the blocking failure occurs on one arm of MMC-1 in which half of the SMs are blocked successfully, the converter status is illustrated in Figure 5-24.

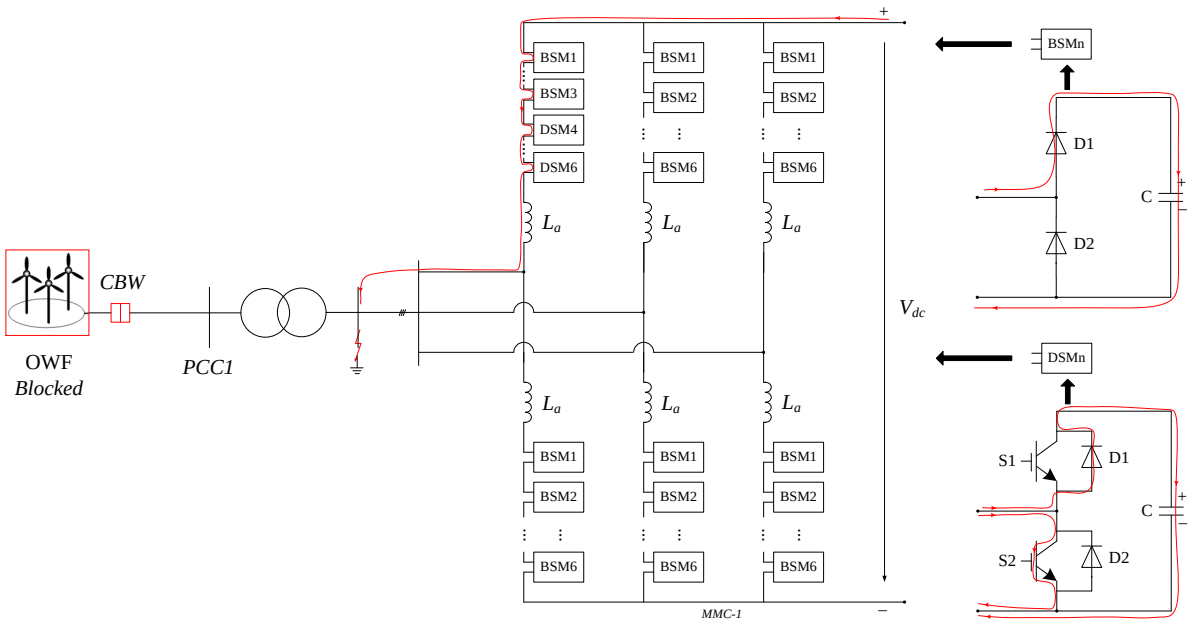


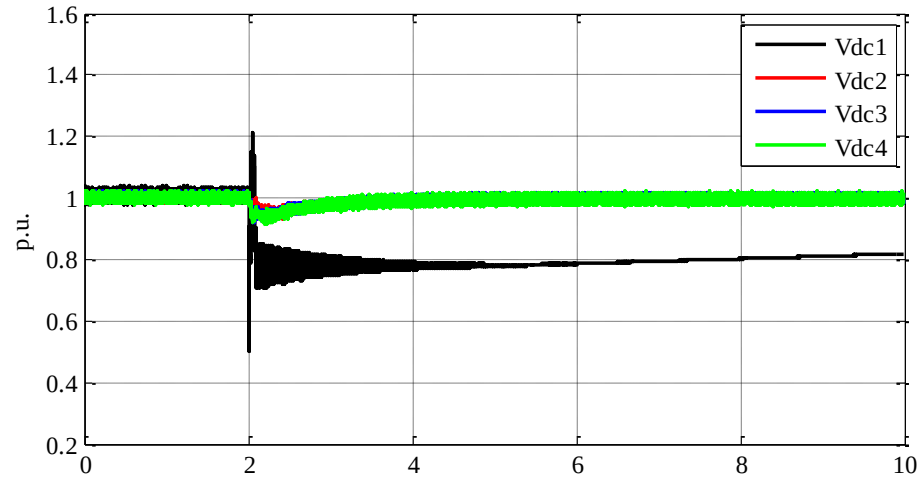
Figure 5-24 System status at T1 with one arm partly blocking failure of MMC-1 in which half of the SMs are blocked successfully

According to the analysis in the previous section, 2 suppositions can be made on the condition of blocking failure discussed in this section: 1) the fault isolation can be achieved using the basic control and protection operation and this condition is non-emergency condition; 2) no/small overvoltage will emerge on the successfully blocked SMs, since half of the SMs on this converter arm are successfully blocked.

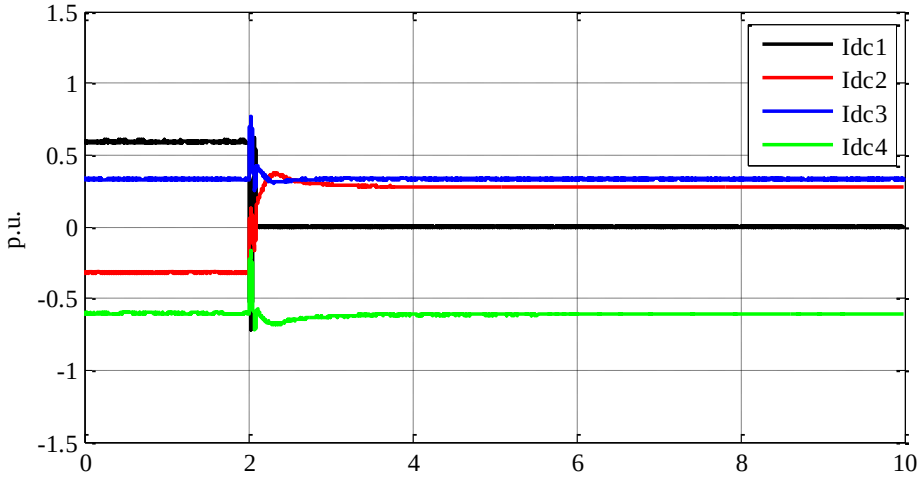
Taking the upper arm of Phase A having blocking failure on half of the SMs as an example, the system performance using the basic control and protection is demonstrated in Figure 5-25: (a) MMC-1 AC-side current in RMS value; (b) DC voltages of the MTDC; (c) DC currents of the MTDC; (d) SM capacitor voltages of the upper arm of Phase A.



(a) Time (s)



(b) Time (s)



(c) Time (s)

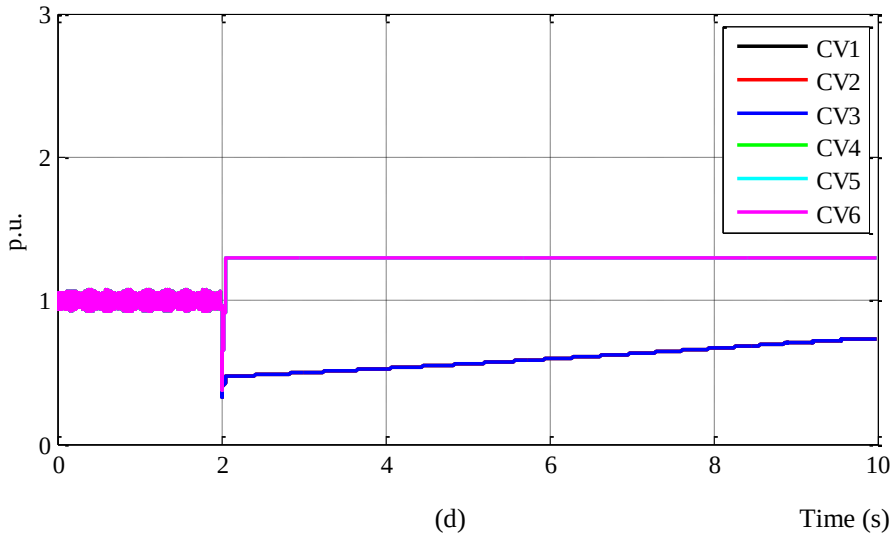


Figure 5-25 System performance under an MMC-1 AC-side fault with one arm of MMC-1 partly blocking failure (half SMs blocked successfully) using the basic control and protection

Figure 5-25(a) demonstrates that the current at MMC-1 AC-side soon decays to 0 after a small current surge following the fault. It indicates the success of the fault isolation. Figure 5-25(b) shows that the DC voltages at the unfaulted terminals are all well maintained after the fault. Figure 5-25(c) shows that the DC currents at the unfaulted terminals do not inject into T1 and the DC current at T1 decays to 0 after the fault. Figure 5-25(d) demonstrates that due to the voltage spikes at MMC-1 DC-side after the fault, there is still small overvoltage emerging on the successfully blocked SMs. However, the overvoltage becomes much smaller than that in Figure 5-23(d), since the increased voltage is squarely divided by 3 blocked SMs.

According to the analysis and simulation results, it can be confirmed that this condition of blocking failure is non-emergency condition for which the special control and protection is not required. However, there is still small overvoltage on the successfully blocked SMs.

5.4.3.3 *One SM blocking failure*

When the blocking failure occurs on one arm of MMC-1 in which only one SM has blocking failure, the converter status is illustrated in Figure 5-26.

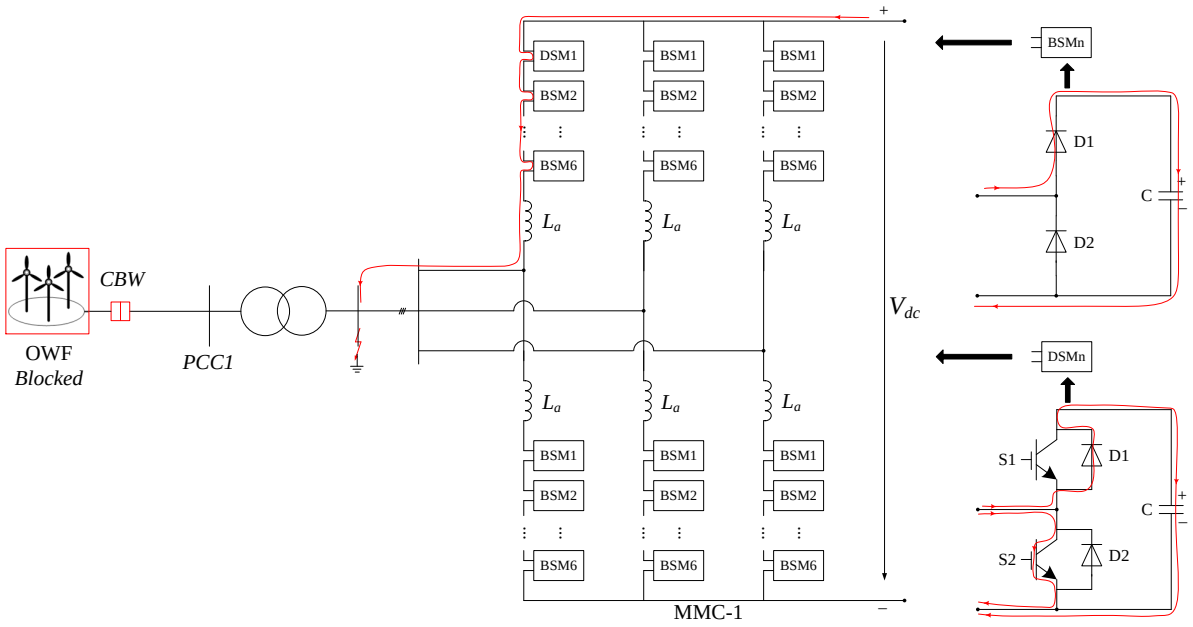


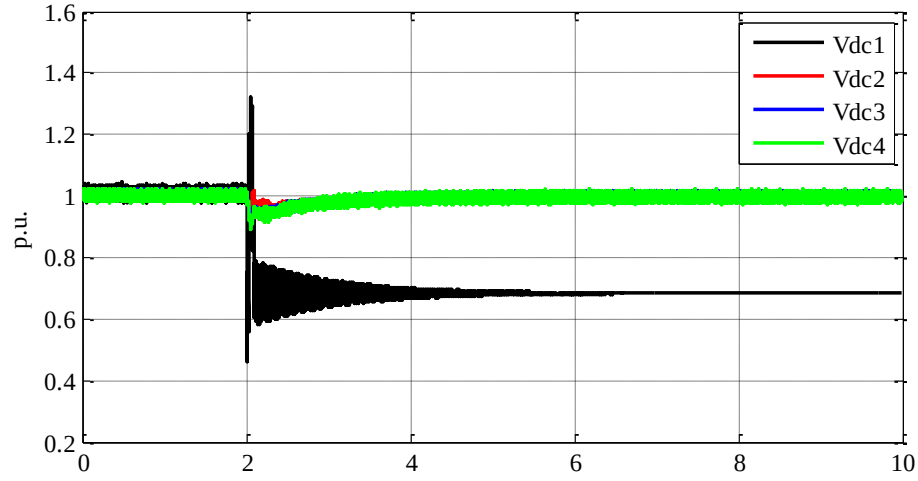
Figure 5-26 System status at T1 with one arm partly blocking failure of MMC-1 in which only 1 SM has blocking failure

According to the analysis and simulation results in the previous 2 sections, it can be supposed that 1) the fault isolation can be achieved using the basic control and protection and this condition of blocking failure is non-emergency condition; 2) no overvoltage will emerge on the successfully blocked SMs.

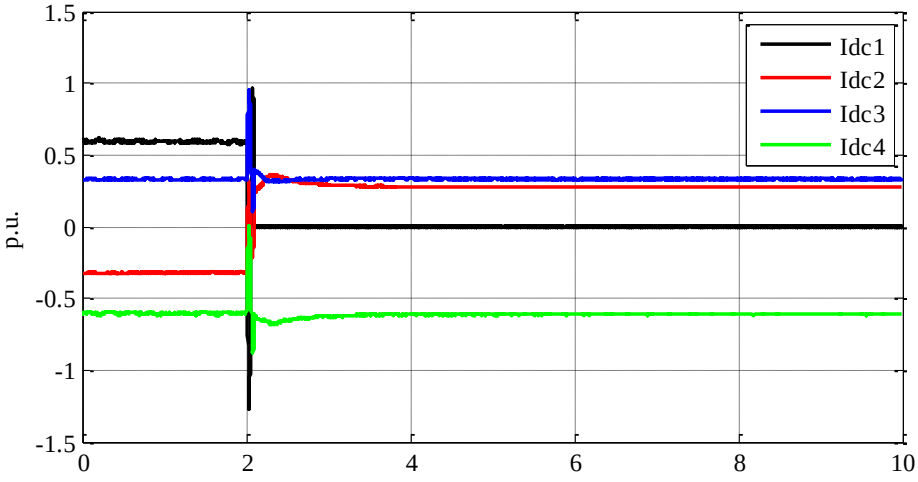
Taking the upper arm of Phase A having the blocking failure on 1 SM as an example, the system performance using the basic control and protection is demonstrated in Figure 5-27: (a) MMC-1 AC-side current in RMS value; (b) DC voltages of the MTDC; (c) DC currents of the MTDC; (d) SM capacitor voltages of the upper arm of Phase A.



(a) Time (s)



(b) Time (s)



(c) Time (s)

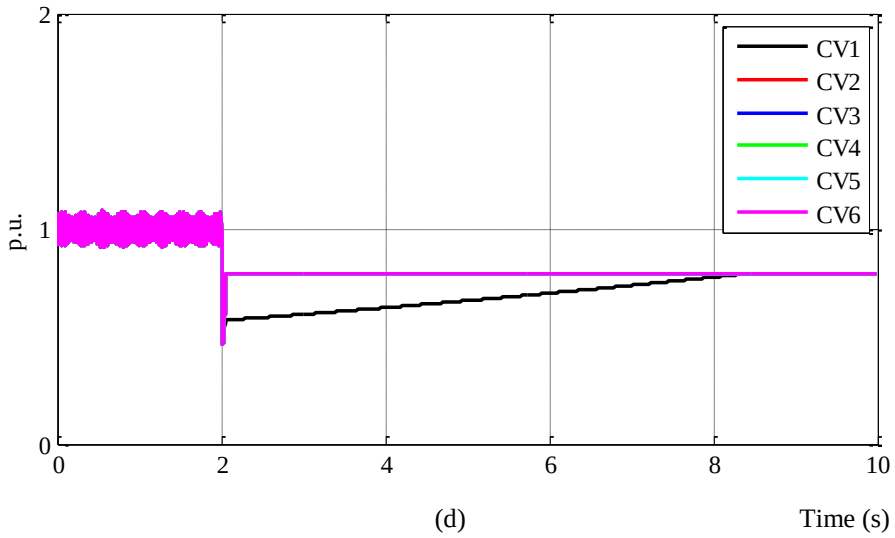


Figure 5-27 System performance under an MMC-1 AC-side fault with one arm of MMC-1 partly blocking failure (1 SM blocked unsuccessfully) using the basic control and protection

Figure 5-27(a) demonstrates that the current at MMC-1 AC-side has a small current surge and it soon decays to 0, which indicates the success of the fault isolation. Figure 5-27(b) shows that the DC voltages at the unfaulted terminals are well maintained. Figure 5-27(c) shows that the DC currents at the unfaulted terminals do not further inject into T1. Figure 5-27(d) demonstrates that the SM capacitor voltages have oscillations before the blocking operation. After the blocking operation, the voltages of the successfully blocked SMs maintain the values at the blocking instant and have no overvoltages.

According to the analysis and simulation results, this condition of blocking failure is non-emergency condition which does not need the special control and protection and there is no potential risk of overvoltage for the successfully blocked SMs. In the discussed 3 conditions of blocking failure, the 3rd condition in which the blocking failure occurs on only 1 SM has the highest possibility. However, it has almost no impact on the system performance using the basic control and protection.

5.4.4 Discussion

The conditions of blocking failure of the faulted-side MMC discussed in Section 5.4 are all assumed the fault occurring at T1. Considering the fault occurring at the other 3 terminals, if the condition is non-emergency condition, the physical isolation of the fault and the faulted section can be achieved using the basic control and protection proposed in Section 5.2. Under the emergency condition, the special control and protection strategy is the same as that proposed in Section 5.4.1.

5.5 Summary

In this chapter, control and protection against AC faults which occur at the MMC AC-side in the MTDC system has been investigated. Two AC fault conditions have been considered respectively. The first condition is that an AC fault occurs at one slave terminal, while the second condition is that an AC fault occurs at the master terminal.

For the fault occurring at one slave terminal, control and protection strategy for the fault isolation and faulted section isolation has been proposed according to the system fault characteristics. Although the control of MMC-3 and MMC-4 has a current limiter, which can effectively limit the fault current, the proposed control and protection strategy is necessary to physically isolate the permanent AC fault. Also, it is valid and can be regarded as a back-up scheme under a transient AC fault when the current limiter does not function or experience other emergency conditions. Since the implementation of the fault isolation does not affect or interrupt the operation of the unfaulted terminals, there is no operation needed for the system recovery.

For the fault occurring at the master terminal, control and protection strategy for the fault isolation and faulted section isolation has been proposed according to the system fault characteristics. However, due to the fact that the implementation of the fault isolation has an impact on and interrupts the operation of the unfaulted terminals, the control and protection strategy for the system recovery has been analysed and proposed. Based on the proposed control and protection strategies, comprehensive control and protection sequences have been proposed respectively for both fault conditions. Simulation case studies have been conducted using the proposed control and protection sequences and the simulation results have proved their effectiveness.

In the previous studies and most published literature, control and protection against AC faults are mostly established under the assumption that the faulted-side MMC can be blocked successfully, which is not always necessarily valid. This chapter has investigated 3 different conditions of blocking failure on the faulted-side MMC after the fault occurs. It includes: 1) the MMC completely fails to be blocked; 2) one converter arm completely fails to be blocked; 3) one converter arm partly fails to be blocked. According to the analysis and simulation results, 1) and 2) have been categorised into emergency condition, necessitating a special control and protection to achieve the fault isolation and faulted section isolation. This chapter has proposed a special control and protection strategy, which can effectively isolate the fault and faulted section. However, potential risks of overcurrent at the AC-side and DC-side of MMC-1 still exist due to the serious condition of converter blocking failure. 3) is considered to be non-emergency condition in which the basic control and protection action can achieve the fault isolation and faulted section isolation. However, if the number of successfully blocked SMs is less than half of the SMs on the converter arm, a potential risk that the successfully blocked SMs may experience being overcharged has been identified.

Since the AC fault investigated in this chapter is permanent, in order to physically isolate the fault, the blocking operation of the faulted-side MMC is proposed. However, if it is a transient fault or the fault current under a permanent fault can be limited, the blocking operation may not be required. Some other approach can be used to ride through the fault. However, it also depends on different fault conditions and system fault characteristics, which can be investigated in the future. In addition, since the design of the MMC model and the control system can affect the system performance, the comparisons of control and protection performance between the current simulation model with other models deserve further investigation.

CHAPTER 6 CONTROL AND PROTECTION OF THE MMC MTDC SYSTEM WITH AN OWF AGAINST DC FAULTS

Control and protection against DC faults in the MMC MTDC system is essential and has always been a challenge. This chapter aims to investigate control and protection schemes against DC fault conditions. The objectives of this chapter are: 1) to study the system fault characteristics under a permanent DC pole-to-pole fault at different locations; 2) to propose the corresponding control and protection scheme at the fault isolation and faulted section isolation stage according to the fault characteristics; 3) to analyse and propose control and protection scheme at the system recovery stage after the faulted section isolation; 4) to synthesise the control and protection scheme at every stage and propose a comprehensive control and protection sequence.

6.1 Introduction

The advantages of the HVDC transmission over HVAC transmission have been generally and widely recognised [3]–[4]. There have been ideas of developing HVDC grids. However, one important issue that restrains the development and scalability of the HVDC grids is effective control and protection against DC faults.

In Chapter 5, it has been described that a complete process of control and protection against a fault generally consists of 5 Phases: Phase 1) fault detection; Phase 2) fault location; Phase 3) fault isolation; Phase 4) faulted section isolation; Phase 5) system recovery, as shown in Figure 5-1. Similar to the research on AC faults in Chapter 5, the research emphasis of control and protection against DC faults is also put from Phase 3 to Phase 5 after the fault location.

6.1.1 Comparison between DC Fault Isolation and AC Fault Isolation

At the fault isolation stage, control and protection against DC faults is much more complex than that against AC faults. This is due to the fact that the system fault characteristics after AC and DC faults are different [35], [55]. When an AC fault occurs on the AC transmission line, normally the AC currents on the AC transmission line have stable zero-crossing points. Hence, the corresponding AC circuit breakers can be controlled and tripped when the current becomes sufficiently small [35]. This largely reduces the requirement of the AC circuit breakers on the mechanical design and manufacturing and their cost. Even if the location of an AC fault is beyond the protection range of AC circuit breakers, the fault isolation can mostly be achieved by blocking the nearby converter station and the current limiter of the converter can also limit the fault current.

For AC faults, AC circuit breakers are predominantly used for the fault isolation. For DC faults, it also intends to use DC circuit breakers to isolate the fault. However, DC currents will increase immediately and significantly after a DC fault occurs and they do not have stable current-crossing-zero point. Therefore, the technology demand, design and manufacturing requirement of the DC circuit breakers and their cost will increase and these have always been challenges in developing the DC circuit breakers. The exploit on the DC circuit breakers has been popular and attractive among all major HVDC equipment suppliers [26], [111], [113] in recent years. Recently, ABB announced that a hybrid DC circuit breaker has been developed [111]. However, it has only been demonstrated and tested on the laboratory voltage scale and has not been proved to be effective under real high-voltage applications. In addition, its expense could be considerable.

6.1.2 DC Fault Isolation Schemes

At present, the control and protection schemes that are widely recognised and approved against DC faults are: 1) install and control of hybrid DC circuit breakers; 2) install and control of DC-DC converters; 3) use and control of full-bridge/hybrid MMCs; 4) use of half-bridge MMCs without additional equipment with associated control and protection strategy after faults.

For Scheme 2), the cost of manufacturing high-power high-voltage DC-DC converters is considerable. In addition, its control logic is complex and its losses have always been a challenge [37]. For Scheme 3), the number of both IGBTs and diodes in a full-bridge MMC are double than that in a same scale half-bridge MMC, which increases the complexity of the control system and the cost of manufacturing and maintenance. For C-MMC, each SM has 3 more IGBTs, 5 more diodes and 1 more capacitor than that of the half-bridge MMC. The increased number of capacitors in each SM increases the volume of the SM and complexity of the control system on balancing the capacitor voltages. In addition, the cost is increased. A comparison of the number of electric components used in the half-bridge, full-bridge and C-MMC is illustrated in Table 6-1 [30] with the assumption that each converter arm has the same number of capacitors so that each capacitor is undertaken with the same voltage under steady-state.

When each capacitor is set to undertake same voltage and the number of capacitor on one arm of the half-bridge MMC, full-bridge MMC and C-MMC is N, the total number of the IGBTs and diodes on one arm of the half-bridge MMC is $2N$; the total number of the IGBTs and diodes on one arm of the full-bridge MMC is $4N$; the total number of the IGBTs and diodes on one arm of the C-MMC is $2.5N$ and $3.5N$, respectively, as shown in Table 6-1.

Table 6-1 Comparison of the Number of Electric Components between Half-bridge MMC, Full-bridge MMC and C-MMC [30]

No. of components on one arm	**Half-bridge MMC**	**Full-bridge MMC**	**C-MMC**
Capacitors	*N*	*N*	*N*
SMs	*N*	*N*	*0.5N*
IGBTs	*2N*	*4N*	*2.5N*
Diodes	*2N*	*4N*	*3.5N*

According to the above analysis, it can be seen that although Scheme 1) − 3) have the capability on the DC fault isolation, they have deficiencies of ① requirement of additional components; ② increased complexity of control logic; ③ increased losses and cost on the additional components and maintenance in comparison with the half-bridge MMC. These 3 schemes could become applicable in practical applications with the development of manufacturing techniques on power electronic devices which lower the losses and cost of the components and they may be widely used in the future. However, before these advanced schemes become commercially available and viable, some operational control and protection schemes should be in place [135]–[136].

The DC fault isolation investigated in this chapter applies Scheme 4). This scheme does not require additional components but needs associated control and protection to achieve the fault isolation. In comparison with the other 3 schemes, the deficiencies of this scheme are that the associated control and protection has an impact on and needs coordinated control of the unfaulted terminals, and has delays during the phase of the system recovery. Nevertheless, it is an economically feasible and reliable solution to achieve the fault isolation. Detailed

control and protection of Scheme 4) on the fault isolation and faulted section isolation will be described in the following sub-sections.

6.1.3 System Recovery after Faulted Section Isolation

In this section, apart from the investigation on the DC fault isolation using Scheme 4), the control and protection strategy at the system recovery phase will also be comprehensively investigated. According to system status after the faulted section isolation of a DC fault, there are 3 important issues to be considered at the system recovery phase: 1) when to initiate the recovery of the unfaulted terminals; 2) at one of the unfaulted terminals, the sequence between deblocking of the MMC and reclosing of the AC circuit breaker; 3) the recovery sequence between the unfaulted terminals. Control and protection sequences at system recovery phase will be proposed. Synthesising the control and protection sequences at the phase of fault isolation, faulted section isolation and system recovery, comprehensive control and protection sequences against DC faults will be proposed.

6.1.4 DC Fault at Different Locations

Another difficult issue on control and protection against DC faults is that DC fault occurs at different locations of the DC grid, which leads to different system fault characteristics. Thus, different corresponding control and protection strategy needs to be applied to isolate the fault. After the fault isolation and faulted section isolation, the system state is various under different fault locations, which leads to different control and protection strategy at system recovery phase.

This chapter investigates 2 DC faults which are both applied as permanent pole-to-pole faults. One of them occurs at T1, which is the power regulated terminal and also the OWF integrated

terminal, while the other fault occurs at T2, which is the master terminal. Section 6.2 and Section 6.3 will investigate these 2 fault conditions respectively. For each fault condition, control and protection at the phase of fault isolation, faulted section isolation and system recovery will be analysed. Corresponding control and protection strategy will be proposed accordingly with comprehensive control and protection sequences proposed. Effectiveness of the proposed control and protection sequences will be finally evaluated using RTDS simulations.

6.2 Control and Protection Against the DC Fault at the Power Regulated Terminal

This section investigates control and protection against a DC fault occurring at the power regulated terminal. T1, T3 and T4 are all such terminals which import/export active power into/from the DC grid. They act as the slave terminals in the MTDC system rather than the master terminal. Although the control of MMC-1 is different with that of MMC-3 and MMC-4 and the direction of the active power transferred of these 3 terminals is not the same, the control and protection strategy against a DC fault at T1 can be generally applicable for that occurring at T3 or T4. In this section, control and protection is analysed for the DC fault occurring at T1.

6.2.1 Fault Characteristics and Fault Isolation

When a DC pole-to-pole fault occurs at T1, the direct impact is on the DC-side voltage and current. For the DC-side voltage, due to a pole-to-pole short-circuit fault, DC voltages at both poles will drop. The DC currents from all terminals will flow into the faulted point leading to large overcurrents in the DC grid. Hence, the main task is to prevent the impact of the DC

overcurrents after the fault occurs.

According to previous analysis, the DC current at each terminal will feed into the faulted point after the fault occurs. The system current status is illustrated in Figure 6-1.

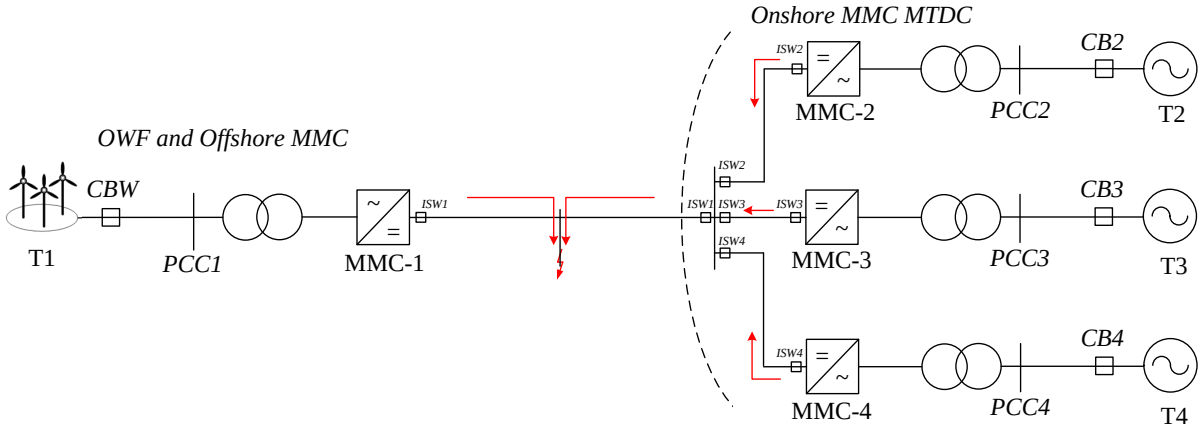


Figure 6-1 DC pole-to-pole fault on DC Cable 1

The DC fault current increases significantly and speedily and its increase rate is much faster than that of the fault current after an AC fault. In order to effectively protect the IGBTs, all the MMCs are blocked swiftly. The system state is illustrated in Figure 6-2.

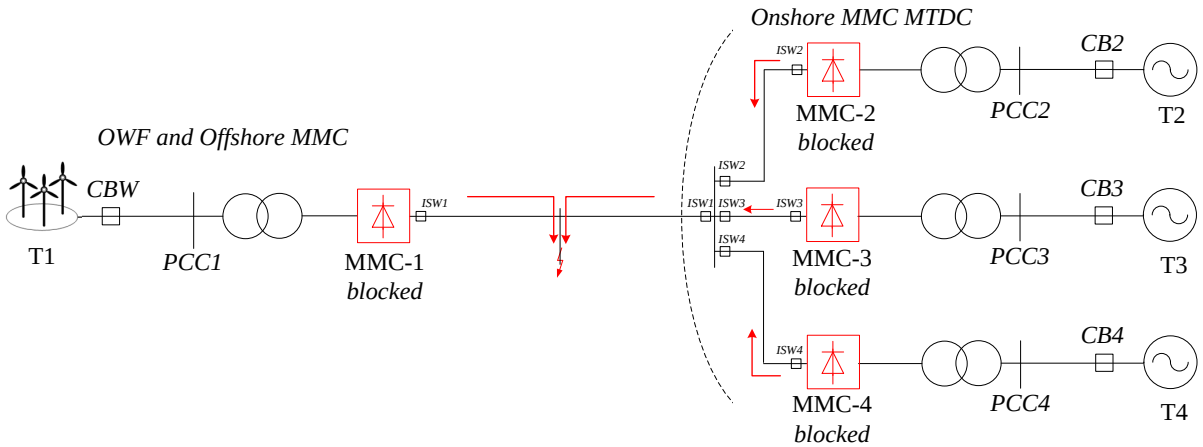


Figure 6-2 System state with blocking all MMCs

Due to the unilateral conductive characteristics of diodes, the currents at the AC-side can still

flow into the DC grid through the MMCs. The red line in Figure 6-3 presents the flow of the phase currents in a blocked MMC.

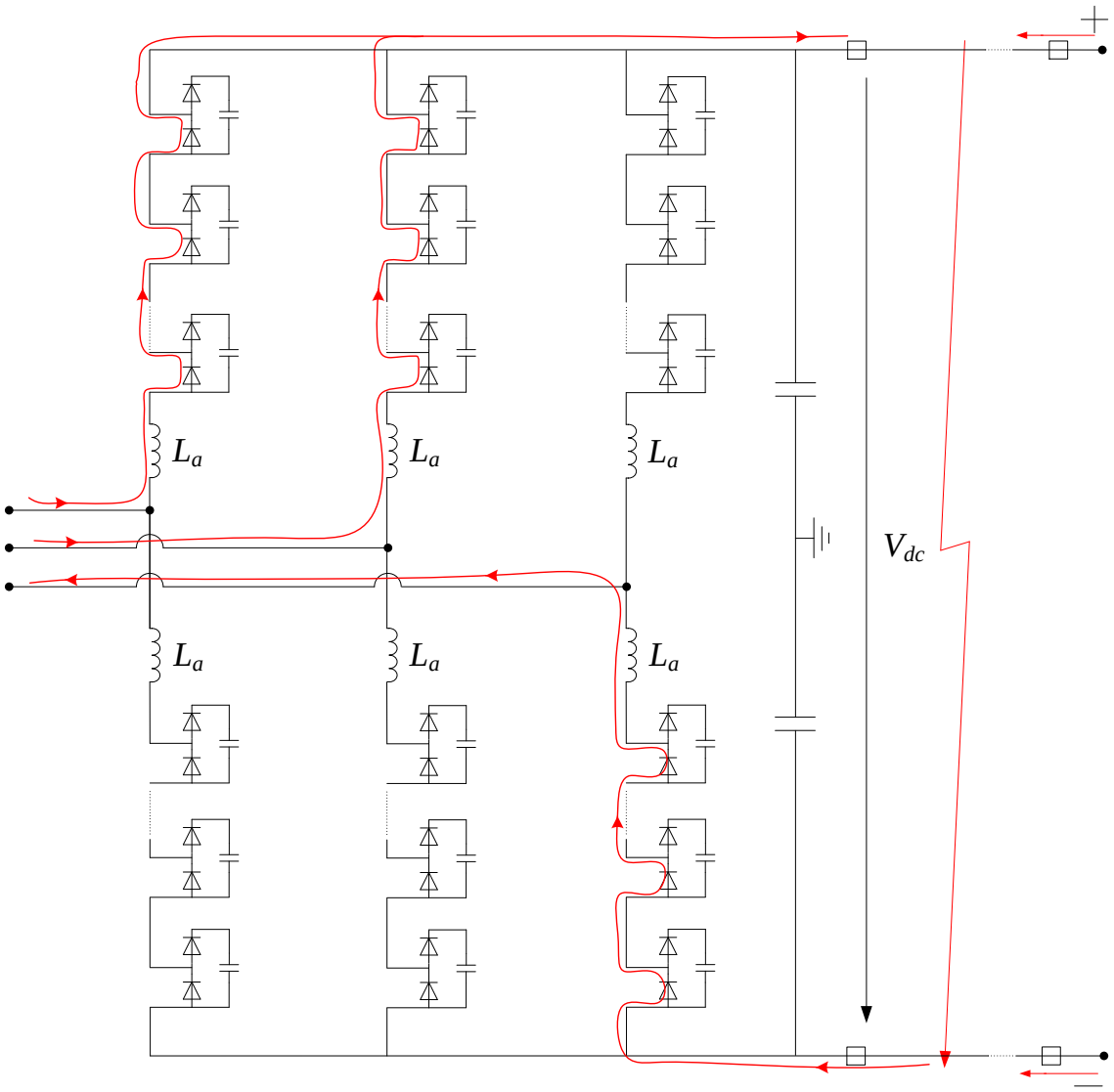


Figure 6-3 Current flow in a blocked MMC under the DC fault

Therefore, in order to isolate the fault, the AC circuit breakers of all the interconnected terminals need to be tripped. In the test system, all the AC circuit breakers including CBW need to be tripped. The current system status is illustrated in Figure 6-4.

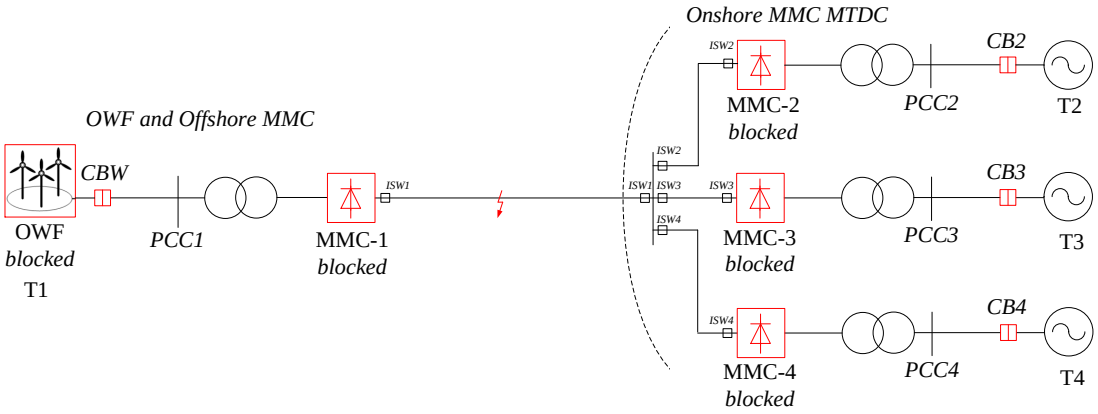


Figure 6-4 System status with fault isolation strategy

The fault isolation is achieved when all the AC circuit breakers are tripped.

6.2.2 Faulted Section Isolation

After the fault isolation, there is no source providing power to the faulted point and DC currents on the DC cable gradually decay to 0. DC *ISW1* will be opened when the current becomes sufficiently small to isolate the faulted section. The system status is illustrated in Figure 6-5.

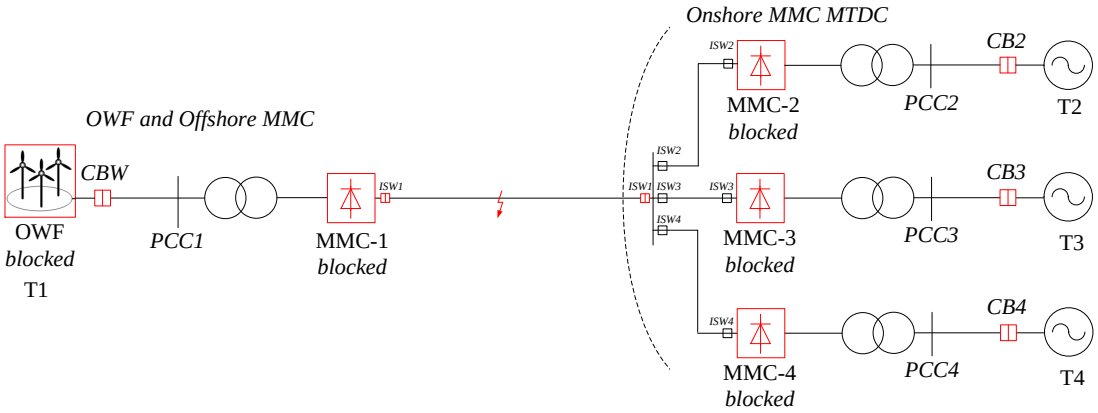


Figure 6-5 System status after faulted section isolation

6.2.3 System Recovery

Since the process of the faulted section isolation necessitates interrupting the operation of the unfaulted terminals, the phase of the system recovery needs to be considered. As for DC cables, the possibility of a fault occurring is much lower than that of DC overhead lines [7], [148]. However, once a fault occurs on a DC cable, it is mostly a permanent fault. Therefore, after the faulted section isolation, the faulted terminal T1 will not resume. Only the unfaulted terminlas T2, T3, T4 will be considered at the system recovery phase. Due to the fact that not only are all the MMCs blocked during the process of the fault isolation, but all the AC circuit breakers are tripped as well, the process of the system recovery needs to consider the deblocking of MMCs and reclosing of AC circuit breakers. According to system status after the faulted section isolation, there are 3 important issues to be considered at the system recovery phase [136]: a) when to initiate the recovery control of the unfaulted terminals; b) at one of the unfaulted terminals, the sequence between deblocking of the MMC and reclosing of the AC circuit breaker; c) the recovery sequence between the unfaulted terminals. Solutions of these 3 issues will form a comprehensive control and protection strategy at the system recovery phase and a control and protection scheme is named for this strategy in practical applications. The following sub-sections will discuss the 3 issues and describe the control and protection scheme.

a. When to Start the Recovery Control

After the faulted section isolation by opening *ISW1*, the DC current on DC Cable 1 decreases to 0. However, the DC currents on the other 3 DC cables are still decreasing with oscillations and have not completely decayed to 0. If the system resumes immediately after the faulted section isolation, large voltage spikes and current surges may emerge. It is more preferable to

start the system recovery control when all DC currents completely decay to 0. Hence, at the system recovery phase, the system recovery control starts with a delay after the faulted section isolation when all DC currents completely decay to 0.

b. Sequence between Deblocking of MMCs and Reclosing of AC Circuit Breakers

As for 1 terminal of the unfaulted terminals, its status before the system recovery control is that the MMC has been blocked and the AC circuit breaker has been tripped. During the process of the system recovery control, it is necessary to consider the issue of the sequence between deblocking of the MMC and reclosing of the AC circuit breaker. In order to analyse this issue, 4 terminals of the MTDC system are divided into 2 categories: one is the terminal, T1, which connects with the OWF and is considered as a terminal with passive AC network, since the restart of the OWF necessitates stable terminal voltage which is provided by external sources; the other one is the terminals, T2, T3 and T4, which connect with AC voltage sources and are considered as terminals with active AC networks, since they have the capability of self-restart. The category principle is similar to that in Section 4 analysing the system start-up control.

The terminal with active AC network is analysed first. If the control and protection sequence is that the MMC is deblocked prior to the reclosing of the AC circuit breaker, this will bring 3 problems: 1) Since the AC circuit breaker has not been reclosed, there is no stable AC voltage at the PCC. Thus, the *dq* decoupled control of the MMC cannot work normally; 2) After deblocking the MMC, all IGBTs start to operate and are no longer under protection. After reclosing the AC circuit breakers, currents will flow through the IGBTs from the AC-side. If there are large inrush currents, the IGBTs may be damaged; 3) Since the MMC is deblocked prior to the reclosing of the AC circuit breaker, the SM capacitors do not experience the pre-

charging process after the fault isolation. Hence, the capacitor voltages before deblocking the MMC may have large difference with their nominal voltages after the deblocking operation, which increases the possibility of current surges after reclosing the AC circuit breakers.

However, if the control and protection sequence is reversed by reclosing the AC circuit breaker prior to the deblocking of the MMC, the above 3 problems may be largely mitigated. 1) After reclosing the AC circuit breaker, the voltage at the PCC will be stabilised, providing the nominal stable AC voltage for the control system of the *dq* decoupled control. Thus, the deblocking of the MMC can work normally afterwards; 2) All the IGBTs are still blocked and protected after reclosing the AC circuit breaker. Currents only flow through the diodes before deblocking the MMC and have no impact on the IGBTs; 3) After reclosing the AC circuit breaker before the deblocking of the MMC, the SM capacitors can have pre-charging process after the faulted isolation. The capacitor voltages will be charged and rise to a stable value which minimises the voltage difference before and after deblocking the MMC and thus reduces the current surges when deblocking the MMC. Therefore, for the terminal with active AC network, the AC circuit breaker should be reclosed prior to the deblocking of the MMC.

For the terminal with a passive AC network, T1, the power source of the AC network is the OWF, the start-up of which requires a stable terminal voltage. Hence, one operation principle of CBW is that CBW will not be close/reclosed until the AC voltage at *PCC1* is nominally established and well stabilised. The AC voltage at *PCC1* is stabilised by the inverting control of MMC-1 which inverts the DC voltage at its DC-side. Therefore, for T1, MMC-1 is deblocked when the DC voltage is well stabilised prior to the reclosing of CBW, and the OWF is deblocked in the end. However, in this case, since the DC fault occurs at T1 and is permanent, the recovery of T1 will not be implemented.

c. Recovery Sequence of Each Terminal

For the MTDC system, the resume of T1 requires stable AC voltage at *PCC1*, which is inverted from the DC voltage at the DC-side of MMC-1, while a stable DC voltage is obtained from the control of the MMCs with active AC networks. Therefore, the terminals with active AC networks are selected to resume prior to the terminal with a passive network. For the terminals with active AC networks, T2 resumes firstly establishing the DC voltage for the DC grid; T3 and T4 will resume in sequence after the resume of T2. Therefore, the general recovery sequence of the MTDC is T2, T3, T4, T1. In this case, since T1 does not resume, the recovery sequence is T2, T3, T4.

d. DARC Scheme

According to the discussion on the above 3 issues, a comprehensive control and protection strategy at the system recovery phase after the faulted section isolation is proposed as follows:

1) The system recovery control starts with a delay when all the DC currents on the DC grid have completely decayed to 0 after the faulted section isolation;
2) The terminals with active AC networks resume prior to the resume of the terminal with a passive AC network;
3) For the terminals with active AC networks, the master terminal with DC voltage control resume prior to the terminals with active power control;
4) For each terminal with an active AC network, the AC circuit breaker is reclosed prior to the deblocking of the MMC;
5) For the terminal with a passive AC network, the MMC is deblocked prior to the reclosing of the AC circuit breaker.

When the control and protection strategy is deployed in practical applications, it is generally named as a control and protection scheme. The control and protection scheme at the system recovery phase is named as Delayed-Auto-Re-Configuration (DARC) scheme. The name of the scheme is explained as follows:

Delayed: As the analysis in Section a, the currents on the DC grid completely decay to 0 with a delay after the faulted section isolation. The system recovery control will start after the delay;

Auto: After the analysis of the above 3 issues, the control and protection strategy at the system recovery phase has been proposed. Based on the proposed control and protection strategy, a comprehensive control and protection sequence can be proposed to realise the automatic recovery control of the unfaulted terminals in practical applications;

Re-Configuration: For DC grids with DC cable models, faults are predominately permanent. Hence, the recovery of the unfaulted terminals necessitates a re-configuration of the original system. In this case, the original 4-terminal system will be finally re-configured into a 3-terminal system.

Figure 6-6 illustrates the process of the DARC scheme.

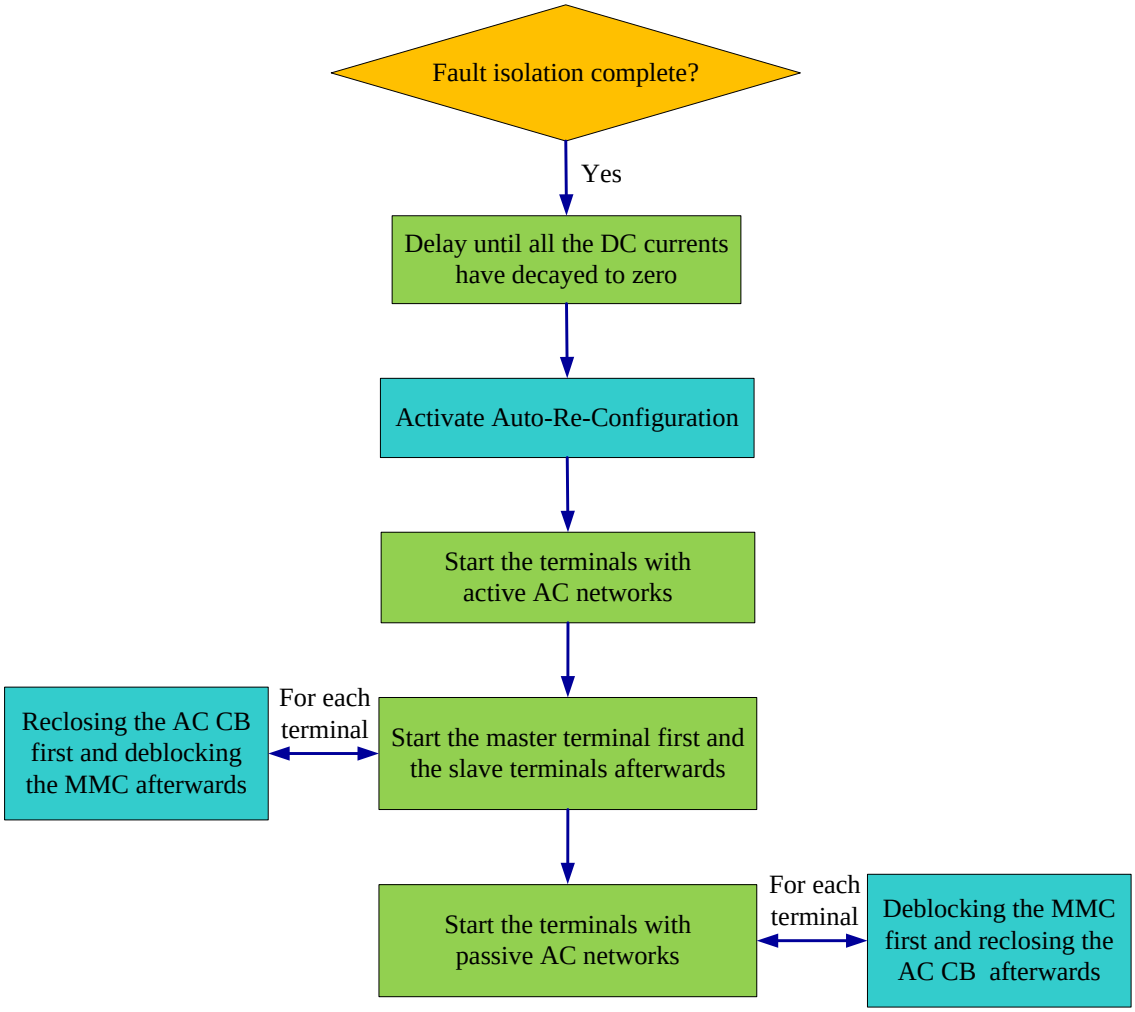


Figure 6-6 Process of DARC scheme

6.2.4 Control and Protection Sequence

Combining the control and protection strategy at the fault isolation phase with that at the system recovery phase, a comprehensive control and protection sequence is proposed in Figure 6-7.

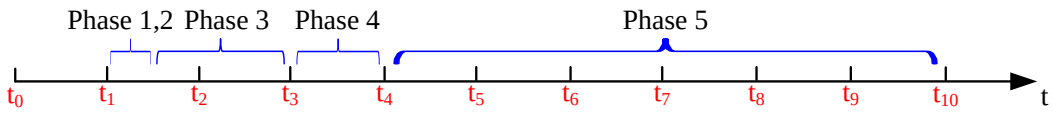


Figure 6-7 Comprehensive control and protection sequence under DC fault on DC Cable 1

According to simulation studies, the DC fault current at T1 increases over 1.2 p.u., which is the assumed current threshold, within 2 ms. Since IGBTs in an MMC can normally be blocked within 2-5 ms after the fault occurs [22], [35], [55], [147], it is assumed that the MMCs are blocked within 2 ms. The AC circuit breaker is assumed to be tripped within 80 ms after the fault. Table 6-2 describes the control action at each instant and the time delay between 2 sequential actions.

Table 6-2 Description of the Control and Protection Sequence in Figure 6-7

t_n	Time	Description	Comment
t_0	0 s	System under normal operation	
t_1	4 s	Apply the DC fault on DC Cable 1	
t_2	4.002 s	Block all MMCs	An MMC can be blocked as fast as 2-5 ms [35], [55], [147];
t_3	4.08 s	Trip all AC *CBs* and *CBW*, block the OWF	An AC CB can generally be tripped within 60-100 ms [35], [55], [147];
t_4	10.7 s	Open *ISW1*	A DC *ISW* can be opened when its current becomes sufficiently small.
t_5	14.7 s	Reclose *CB2*	A delay of 2 s is set between two sequential control actions. This delay can be shortened as long as the system reaches a steady condition after the former control action.
t_6	16.7 s	Deblock MMC-2	
t_7	18.7 s	Reclose *CB3*	
t_8	20.7 s	Deblock MMC-3	
t_9	22.7 s	Reclose *CB4*	
t_{10}	24.7 s	Deblock MMC-4	

The comprehensive control and protection sequence includes the phase of fault isolation, faulted section isolation and system recovery. The system state after the recovery of the unfaulted terminals is illustrated in Figure 6-8.

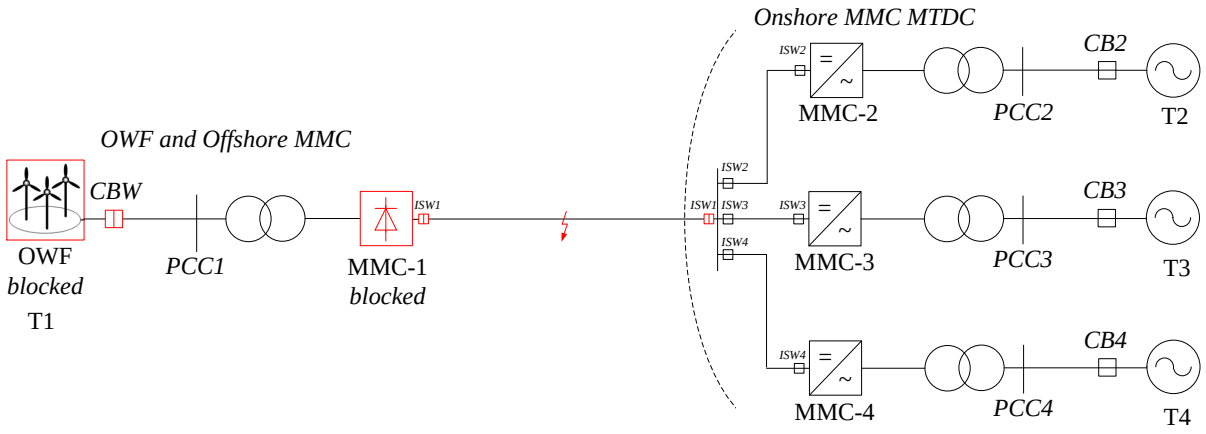


Figure 6-8 System state after the recovery of the unfaulted terminals

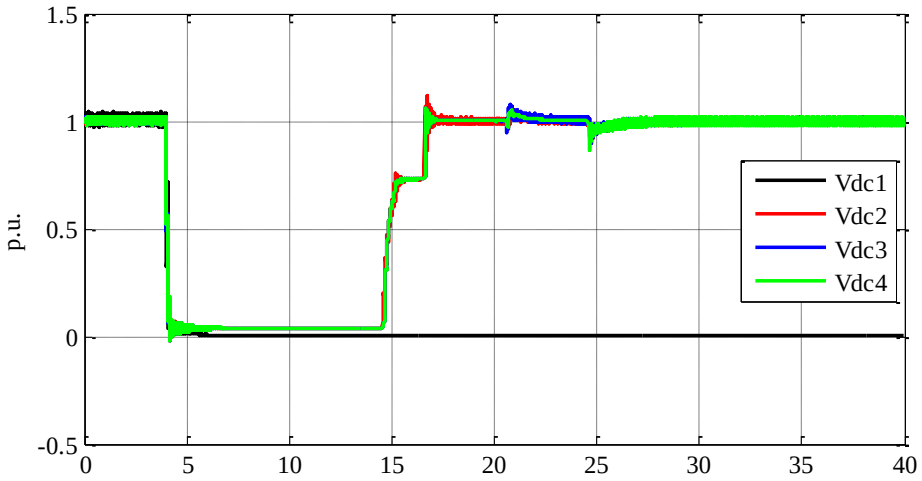
Figure 6-8 shows that after the complete control and protection action, the faulted section has been effectively isolated and the 4-terminal system is finally reconfigured into a 3-terminal system.

6.2.5 Simulation Case Study

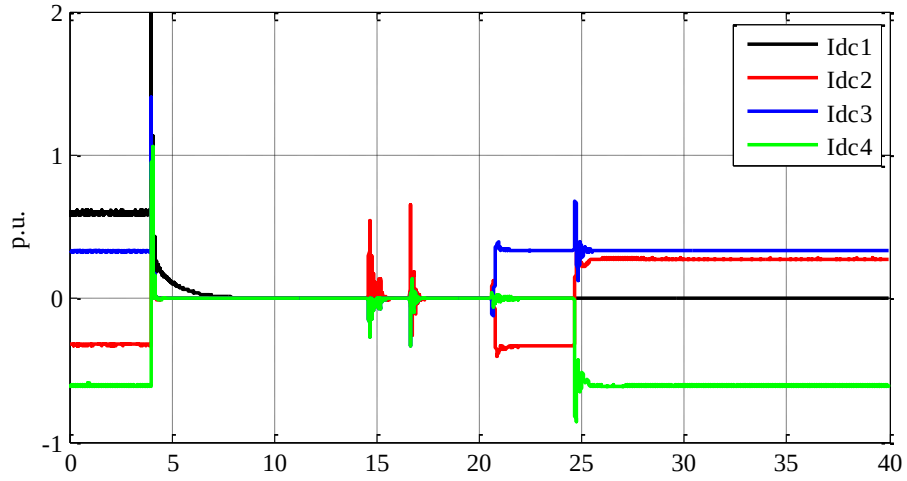
The system performance using the proposed control and protection sequence is demonstrated in Case A. In Case B, the control and protection sequence at the phase of fault isolation and faulted section isolation applied is the same as that in Case A, while a different control and protection sequence at the system recovery phase is used.

6.2.5.1 Case A

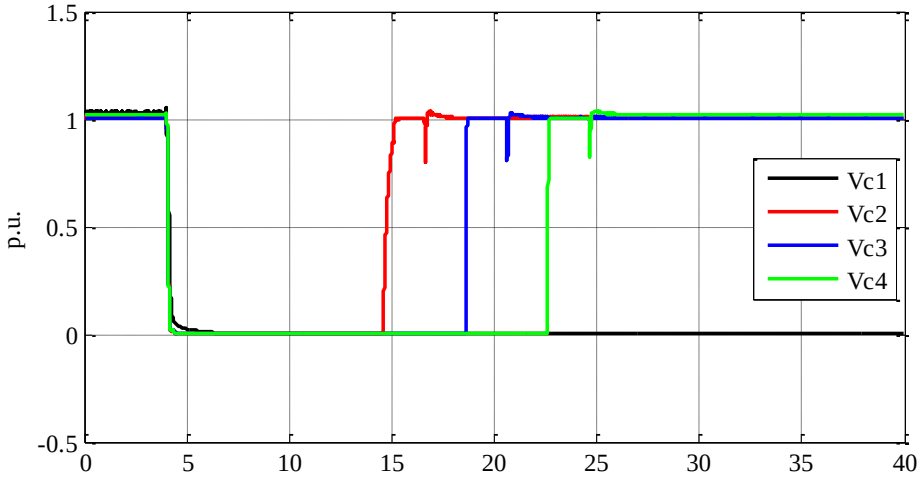
The fault is applied at 4 s on DC Cable 1 as a permanent pole-to-pole fault. The system performance using the proposed control and protection sequence in Section 6.2.4 is demonstrated in Figure 6-9: (a) DC voltages of the MTDC; (b) DC currents of the MTDC; (c) MMC AC-side voltages in RMS value; (d) MMC AC-side currents in RMS value; (e) active power; (f) reactive power.


1.5
1
0.5
0
-0.5
p.u.
0
5
10
15
20
25
30
35
40
Vdc1
Vdc2
Vdc3
Vdc4
Time (s)

(a)


2
1
0
-1
p.u.
0
5
10
15
20
25
30
35
40
Idc1
Idc2
Idc3
Idc4
Time (s)

(b)


1.5
1
0.5
0
-0.5
p.u.
0
5
10
15
20
25
30
35
40
Vc1
Vc2
Vc3
Vc4
Time (s)

(c)

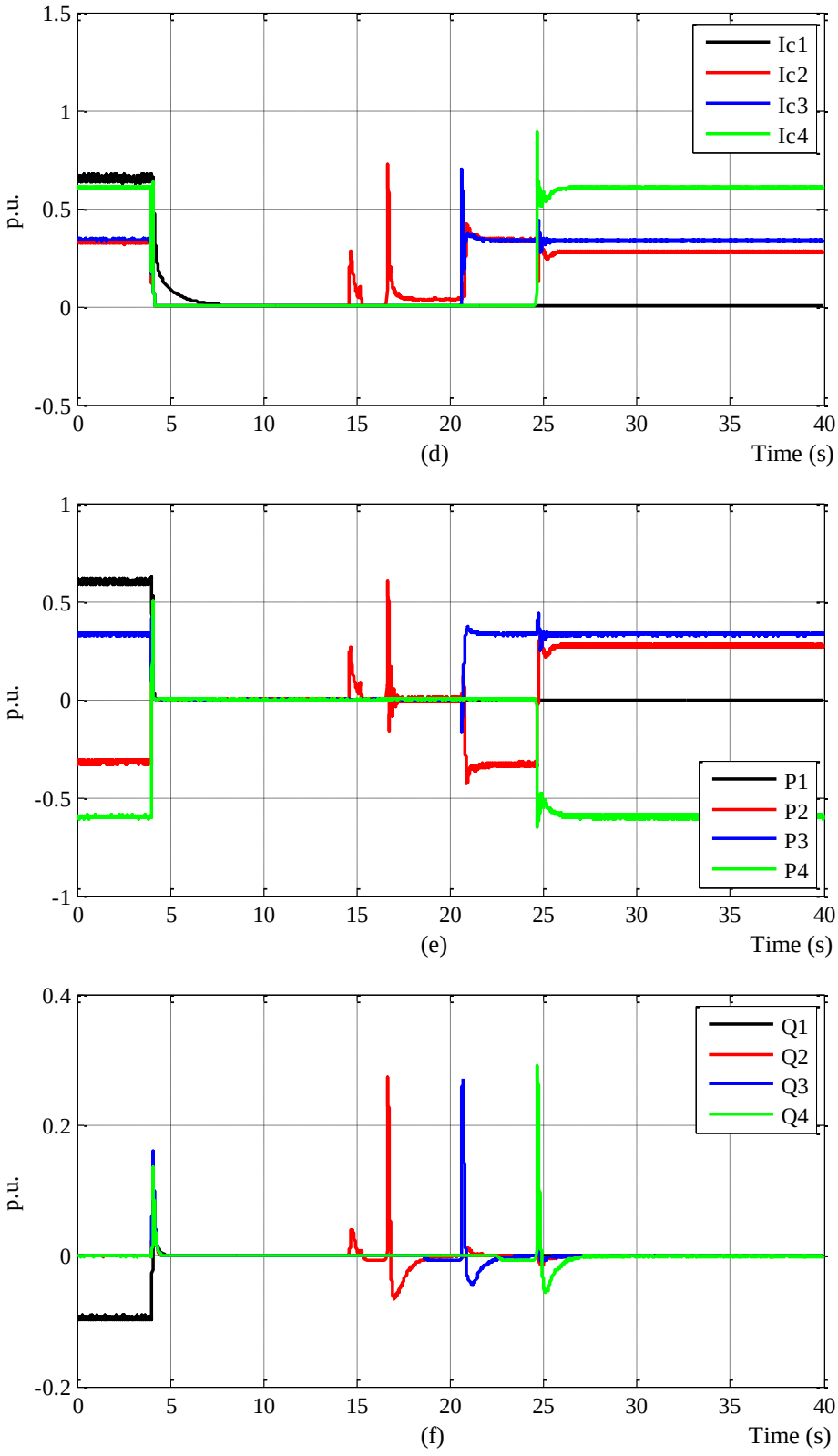


Figure 6-9 System performance under an DC fault on DC Cable 1 using proposed control and protection sequence

Figure 6-9(a) demonstrates that the DC voltages drop after the fault isolation with no significant oscillations. The system recovery control starts at 14.7 s. The DC voltage of the MTDC is established by MMC-2 and is well maintained afterwards. DC overcurrent can be observed after the fault in Figure 6-9(b). Due to effective fault isolation, DC currents at 4 terminals gradually decrease and completely decay to 0 at around 14.7 s. During the system recovery phase, DC currents at the unfaulted terminals resume smoothly with small current surges. Figure 6-9(c) demonstrates that due to effective fault isolation, MMC AC-side voltages decrease to 0 with no significant oscillations. During the system recovery phase, the MMC AC-side voltages at T2, T3, T4 resume stably in sequence. Figure 6-9(d) shows that during the system recovery phase, the MMC AC-side currents at T2, T3, T4 resume in sequence with small current surges, which are all smaller than 1 p.u.. Due to effective fault isolation, the active power at each terminal soon decreases to 0 after the fault as shown in Figure 6-9(e). The active power of the unfaulted terminals starts to resume at 14.7 s and resume in sequence smoothly. Figure 6-9(f) shows that due to effective control and protection action, only small oscillations of reactive power emerge during the whole process.

Therefore, the simulation results prove the effectiveness of the proposed control and protection sequence. The fault and the faulted section are effectively isolated. The unfaulted terminals resume operation smoothly thanks to the effective DARC scheme.

6.2.5.2 Case B

In order to demonstrate the usefulness of the DARC scheme and the importance of the control and protection sequence at the system recovery phase, a comparison case study is conducted. In this case, the recovery sequence of the unfaulted terminals is T3, T4, T2, while the control and protection sequence at the phase of fault isolation and faulted section isolation is the same

as that in Case A. Detailed control and protection sequence is presented in Figure 6-10. Table 6-3 describes the control action at each instant and the delay between 2 sequential actions.

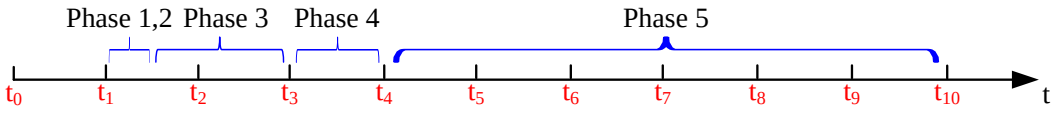


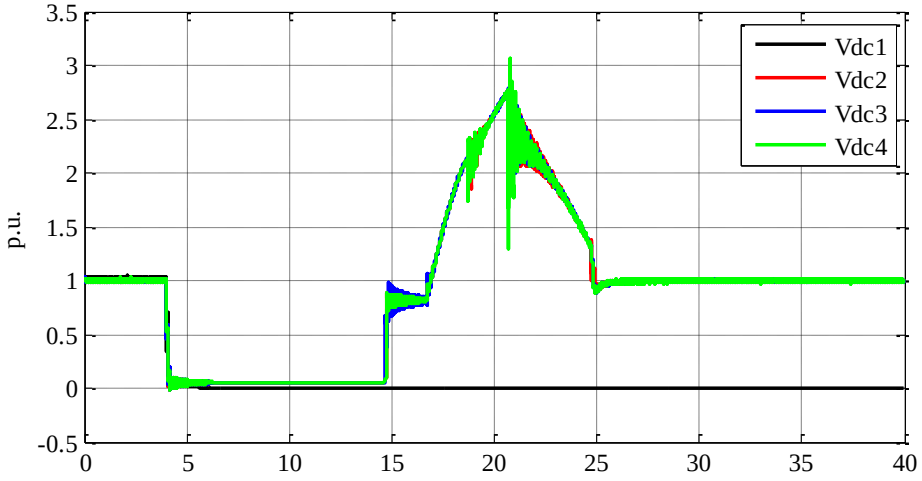
Figure 6-10 Different control and protection sequence under DC fault on DC Cable 1

Table 6-3 Description of the Control and Protection Sequence in Figure 6-10

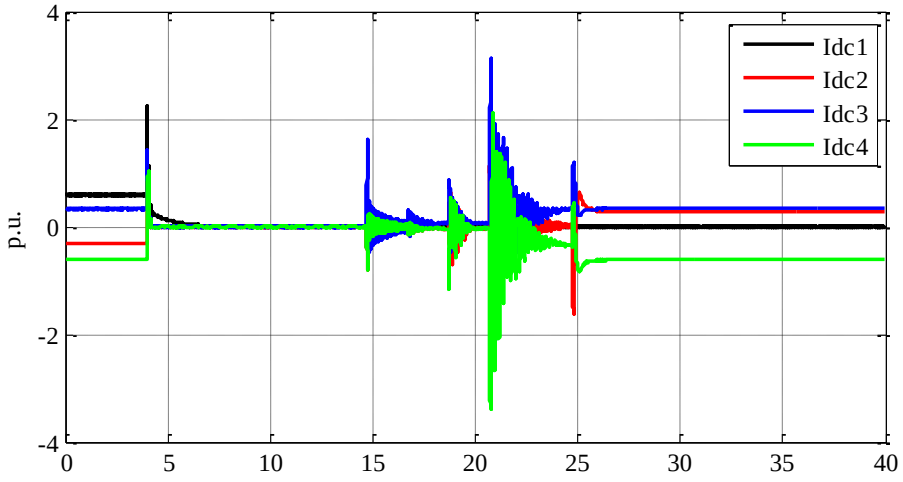
t_n	Time	Description	Comment
t_0	0 s	System under normal operation	
t_1	4 s	Apply the DC fault on DC Cable 1	
t_2	4.002 s	Block all MMCs	An MMC can be blocked as fast as 2-5 ms;
t_3	4.08 s	Trip all AC *CBs* and *CBW*, Block the OWF	An AC CB can generally be tripped within 60-100 ms;
t_4	10.7 s	Open *ISW1*	A DC *ISW* can be opened when its current becomes sufficiently small;
t_5	14.7 s	Reclose *CB3*	A same delay of 2 s is set between two sequential control actions. However, the recovery sequence of each terminal becomes T3, T4, T2.
t_6	16.7 s	Deblock MMC-3	
t_7	18.7 s	Reclose *CB4*	
t_8	20.7 s	Deblock MMC-4	
t_9	22.7 s	Reclose *CB2*	
t_{10}	24.7 s	Deblock MMC-2	

The system performance using the above control and protection sequence is demonstrated in Figure 6-11: (a) DC voltages of the MTDC; (b) DC currents of the MTDC; (c) MMC AC-side voltages in RMS value; (d) MMC AC-side currents in RMS value; (e) active power; (f)

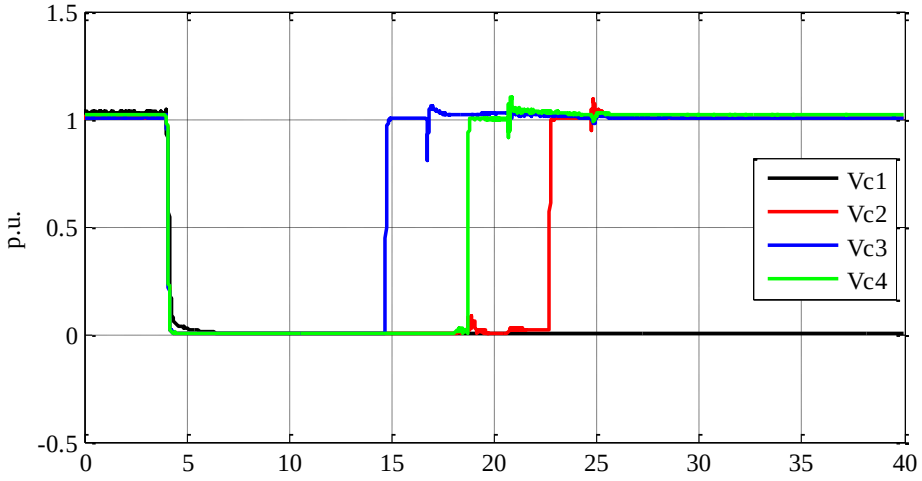
reactive power.



(a)



(b)



(c)

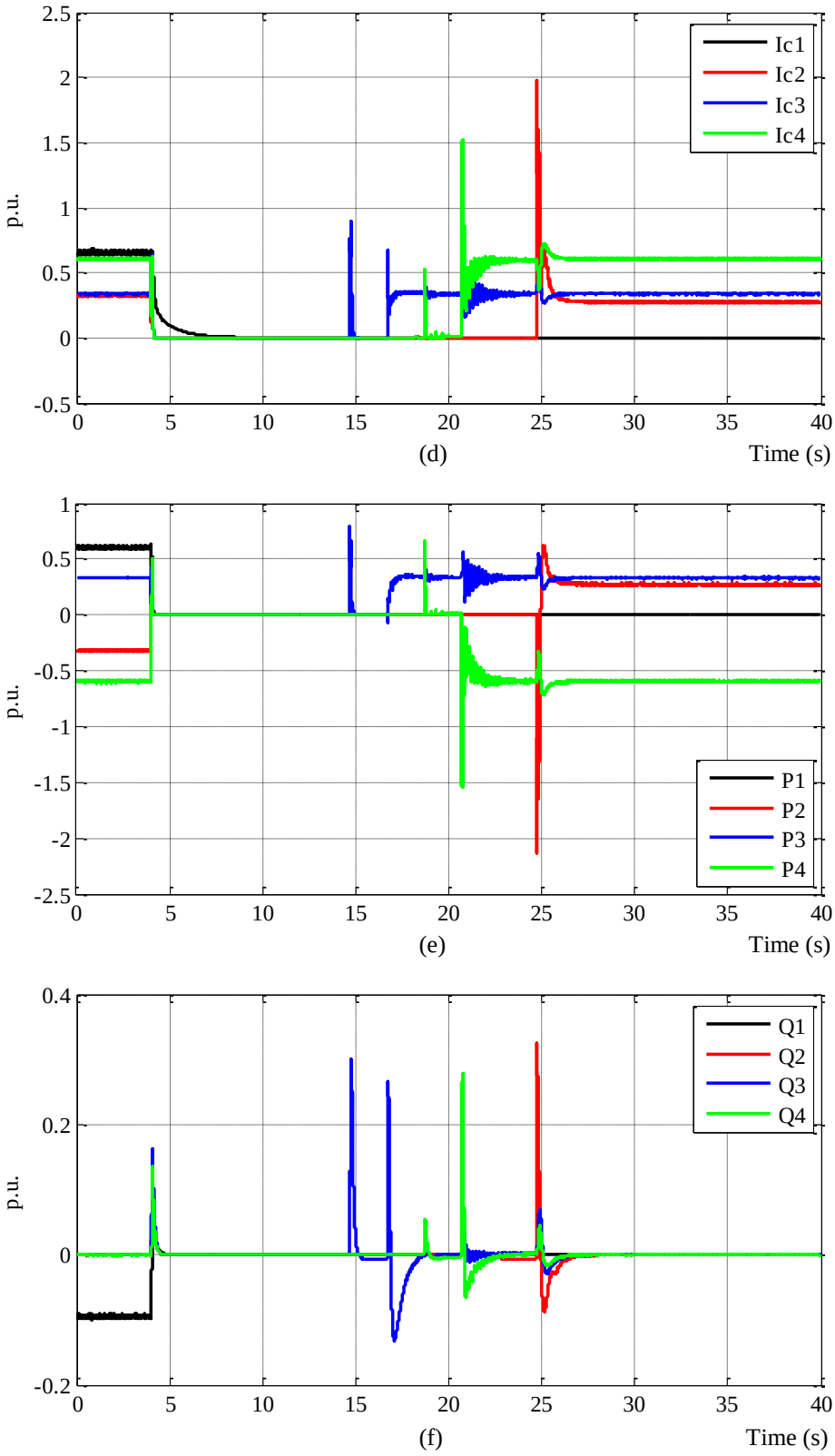


Figure 6-11 System performance under an DC fault on DC Cable 1 using a different control and protection sequence at the system recovery phase

Due to the fact that the control and protection sequence at the phase of fault isolation and faulted section isolation is the same as that in Case A, the following discussion only focuses on the system performance at the system recovery phase. Figure 6-11(a) demonstrates that DC voltages resume to the nominal state at 24.7 s. However, the voltage oscillations are more significant than those in Figure 6-9(a), since the DC voltage has not been completely established until the resume of T2. Large fluctuations and inrush currents can be observed in Figure 6-11(b), particularly at 20.7 s when MMC-4 is deblocked. However, in Figure 6-9(b), the recovery of the DC currents is smooth and stable. This is because of the control and protection sequence at the system recovery phase: In this case, T3 and T4, which are both power regulated terminals, which resume prior to the resume of the DC voltage controlled terminal, T2. That is to say, the resume of active power occurs when the DC voltage has not been completely established at the nominal condition. Large overcurrents at MMC AC-side can be observed in Figure 6-11(d), particularly at the instant when MMC-4 and MMC-2 are deblocked, since T3 and T4 resume prior to the resume of T2. In comparison with the performance shown in Figure 6-9(e), large oscillations of the active power are shown in Figure 6-11(e). The most significant oscillations emerge at 24.7 s when T2 resumes. This is because the resume of T2 is affected by T3 and T4, which have both resumed and transferred power in the DC grid under the condition that the DC voltage has not been nominally established.

Therefore, from the comparisons of the system performance between Case A and Case B, it can be seen that the proposed DARC scheme is more appropriate and can resume the system in a smooth and stable manner.

Control and protection investigated in this section is for DC faults which occur at one of the

slave terminals. The analysis is carried out taking a fault occurring at T1 as an example. When the faults at T3 or T4, which are also slave terminals, the proposed control and protection strategy can also be applicable and the proposed control and protection sequence can be similarly applied.

6.3 Control and Protection Against the DC Fault at the Master Terminal

This section investigates control and protection against a DC fault occurring at the master terminal, T2, which maintains the DC voltage of the MTDC. When a fault occurs at this terminal, the process of control and protection becomes more complex, especially during the system recovery phase. Similar to that in the previous section, the DC fault is also applied as a permanent pole-to-pole fault.

6.3.1 Fault Characteristics and Fault Isolation

When the fault occurs on DC Cable 2, DC voltages at both poles will drop and DC currents will flow into the faulted point. If there is no associated control and protection operation applied, currents will continue flowing into the faulted point from all adjacent AC network through the MMCs. The system fault characteristics are similar to those analysed in Section 6.2.1 when the fault occurs on DC Cable 1. The current system status is illustrated in Figure 6-12.

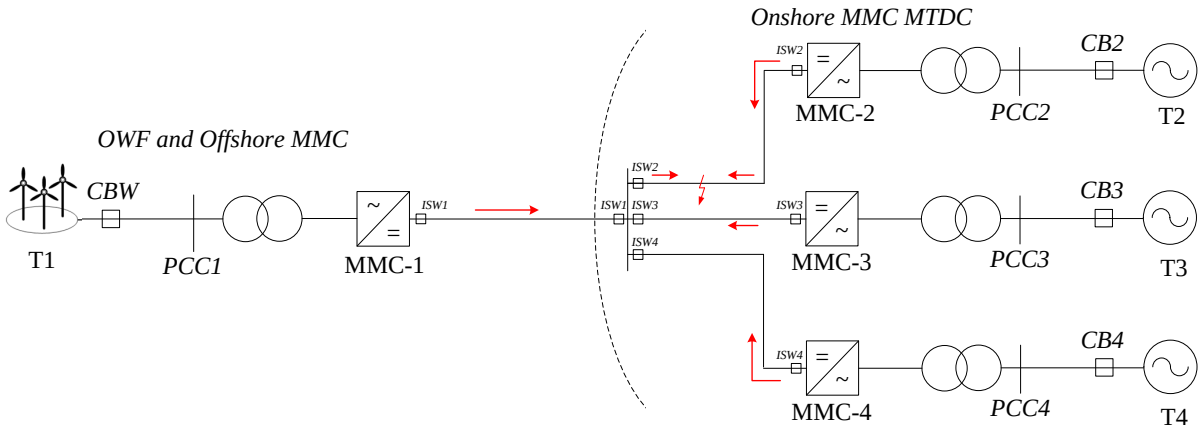


Figure 6-12 DC pole-to-pole fault on DC Cable 2

The fault isolation strategy is similar to that applied in Section 6.2.1. Firstly, all MMCs are swiftly blocked to protect the IGBTs and the MMCs become uncontrolled rectifier with diode bridge. Since the fault occurs on the DC grid, the currents on the AC networks can still flow to the DC-side through the diodes. Hence, the AC circuit breakers including CBW at all adjacent terminals need to be tripped to isolate the fault. The OWF is blocked at the same instant when CBW is tripped. The system state is illustrated in Figure 6-13.

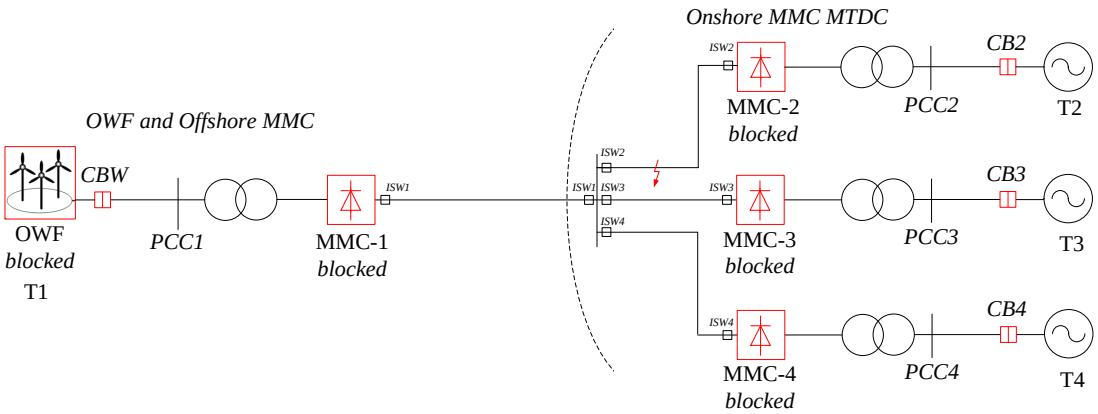


Figure 6-13 System state with fault isolation strategy

The fault isolation is achieved when all AC circuit breakers are tripped.

6.3.2 Faulted Section Isolation

After the fault isolation, DC currents on the DC grid start to decrease and DC *ISW2* is opened when the current becomes sufficiently small to isolate the faulted section. The faulted section isolation strategy is also similar to that applied in Section 6.2.2. The current system state is illustrated in Figure 6-14.

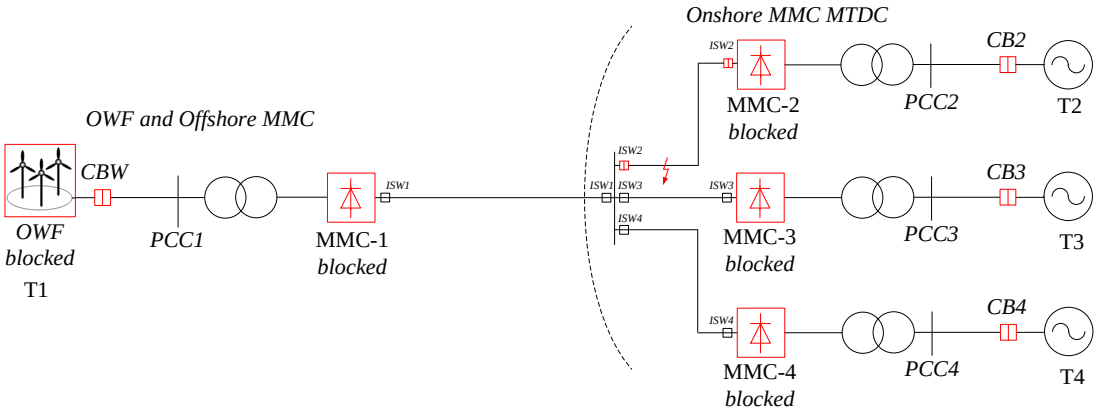


Figure 6-14 System state after the faulted section isolation

6.3.3 System Recovery

Since the fault occurs at T2 and is permanent, T2 will not resume after the faulted section isolation. Similar to those in Section 6.2.3, the same 3 issues are considered during the system recovery phase. Based on the solutions of these issues, a DARC scheme can be formed for the system recovery control.

a. When to Start the Recovery Control

After DC *ISW2* being opened, the DC current on DC Cable 2 becomes 0. However, the DC currents on the other 3 DC cables are still decreasing without completely decaying to 0. Similar to the solution in Section 6.2.3a, the system recovery control will start when all DC

currents in the MTDC grid have completely decayed to 0, so as to reduce the voltage spikes and current surges during the recovery process.

b. Sequence between Deblocking of MMCs and Reclosing of AC Circuit Breakers

According to the discussion in Section 6.2.3b, for the terminals with active AC networks, T3 and T4, the AC circuit breaker is reclosed prior to the deblocking of the MMC; for the terminal with a passive AC network, T1, MMC-1 is deblocked prior to the reclosing of the AC circuit breaker, CBW. The OWF is deblocked in the end after the reclosing of CBW.

c. Recovery Sequence of Each Terminal

According to the discussion in Section 6.2.3c, the terminals with active AC networks resume prior to the resume of the terminal with a passive AC network. Among the terminals with active AC networks, the terminal with DC voltage control resume prior to the terminal with active power control. However, in this case, the DC voltage controlled terminal, T2, will not resume due to the permanent fault. Hence, if the unfaulted terminals are required to resume, one of the active power controlled terminals, T3 and T4, needs to take over the control of DC voltage. In this case, T4 is selected to switch the control mode from active power control to DC voltage control. Therefore, the recovery sequence of the unfaulted terminals is T4, T3, T1.

d. DARC Scheme

Based on the discussions on the above 3 issues, a comprehensive control and protection strategy at the system recovery phase can be proposed under the DC fault at the master terminal. The proposed strategy has 5 principles in which 1), 2), 4), 5) are identical to those proposed in Section 6.2.3d and only 3) needs to be modified.

3) For the terminals with active AC networks, the master terminal with DC voltage control resume prior to the terminals with active power control; when the master terminal cannot resume, one of the terminals with active power control needs to switch control mode to take over the DC voltage control and resume prior to the resume of the other terminals;

As described in Section 6.2.3d, when this strategy is deployed in real applications, it is called a DARC scheme. Compared with the former DARC scheme, this scheme has a modification and can be called a modified DARC scheme, the process of which is illustrated in Figure 6-15.

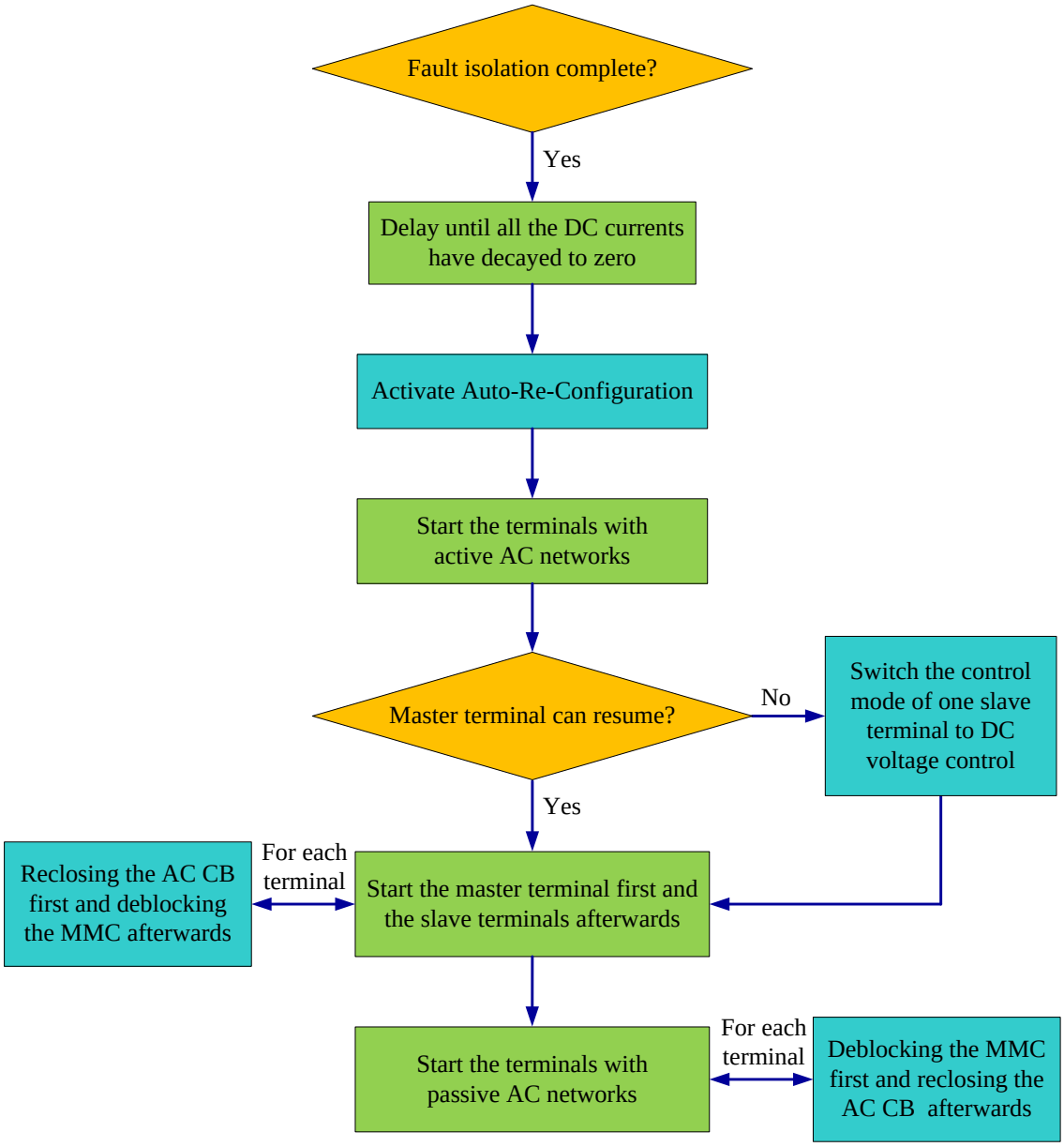


Figure 6-15 Process of modified DARC scheme

The application of the modified DARC scheme may require one terminal to switch control mode during the system reconfiguration process. This is because master-slave control is applied and the fault occurs at the master terminal and is permanent. In order to resume the unfaulted terminal, the switching of control mode is inevitable.

6.3.4 Control and Protection Sequence

Combining the control and protection strategy at the phase of fault isolation, faulted section isolation and system recovery, a comprehensive control and protection sequence against the DC fault at the master terminal is proposed in Figure 6-16.

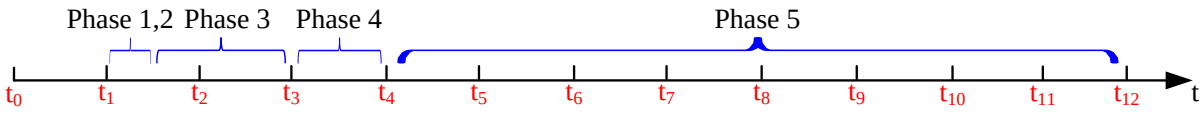


Figure 6-16 Comprehensive control and protection sequence under DC fault on DC Cable 2

According to simulation studies, the DC fault current at T1 increases over 1.2 p.u., which is the assumed current threshold, within 2 ms. Hence, MMCs are assumed to be blocked within 2 ms. The AC circuit breaker is assumed to be tripped within 80 ms after the fault. Table 6-4 describes the control action at each instant and the delay between 2 sequential actions.

Table 6-4 Description of the Control and Protection Sequence in Figure 6-16

t_n	Time	Description	Comment
t_0	0 s	System under normal operation	
t_1	4 s	Apply the DC fault on DC Cable 2	
t_2	4.002 s	Block all MMCs	An MMC can be blocked as fast as 2-5 ms;
t_3	4.08 s	Trip all AC *CBs* and *CBW*, block the OWF	An AC CB can generally be tripped within 60-100 ms;
t_4	4.17 s	Open *ISW2*	A DC *ISW* can be opened when its current becomes sufficiently small;
t_5	8.17 s	Change control mode of MMC-4 to DC voltage control	A delay of 2 s is set between two sequential control actions. This delay

t_6	10.17 s	Reclose *CB4*	can be shortened as long as the system reaches a steady condition after the former control action.
t_7	12.17 s	Deblock MMC-4	
t_8	14.17 s	Reclose *CB3*	
t_9	16.17 s	Deblock MMC-3	
t_{10}	18.17 s	Deblock MMC-1	
t_{11}	24.17 s	Reclose *CBW*	The re-integration of the OWF needs a stable AC voltage at *PCC1*. Hence, a long delay of 6 s is chosen.
t_{12}	25.17 s	Deblock *OWF*	

The proposed control and protection sequence consists of the fault isolation, faulted section isolation and system recovery, in which the switching of control mode of T4 is included. The system status after the resume of the unfaulted terminals is illustrated in Figure 6-17.

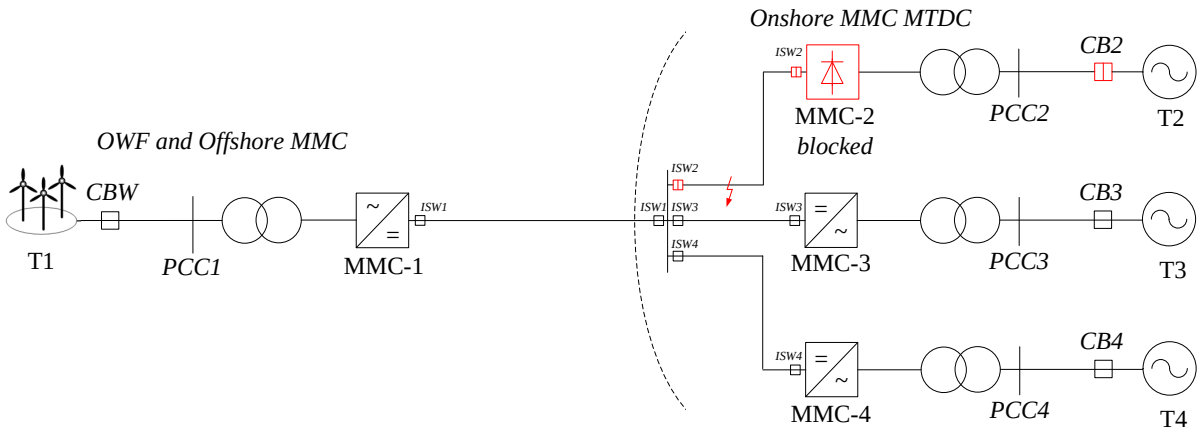


Figure 6-17 System state after the recovery of the unfaulted terminals

Figure 6-17 shows that with the proposed control and protection strategy, the faulted section is effectively isolated. Although the master terminal cannot resume after the faulted section isolation, with effective adjustment of control mode of T4, the resume of the unfaulted

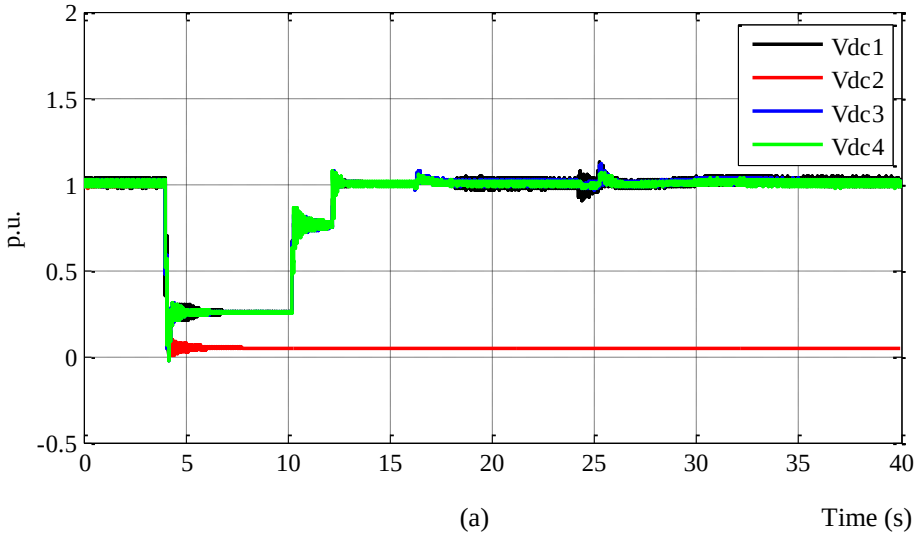
terminals is achieved and the system will be finally reconfigured into a 3-terminal system.

6.3.5 Simulation Case Study

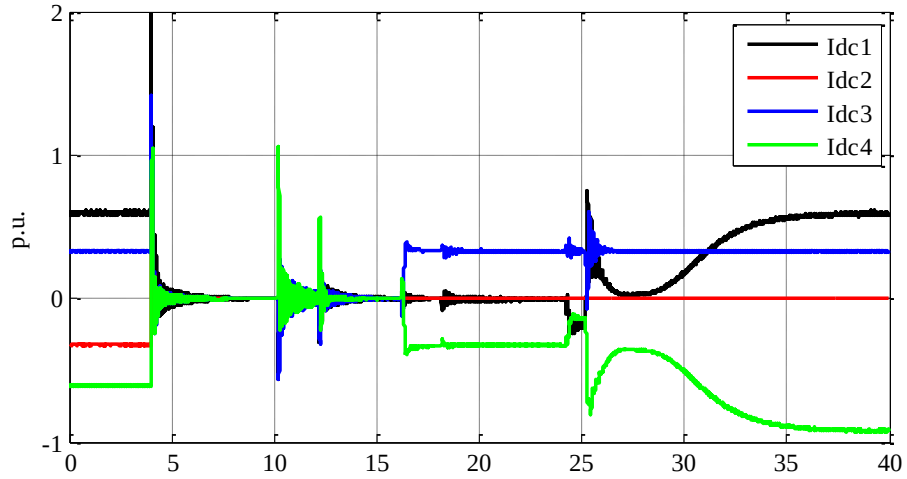
The system performance using the proposed control and protection sequence is demonstrated in Case A. In Case B, a control and protection scheme for the MTDC system with coordinated droop control is discussed and a corresponding control and protection sequence is proposed.

6.3.5.1 Case A

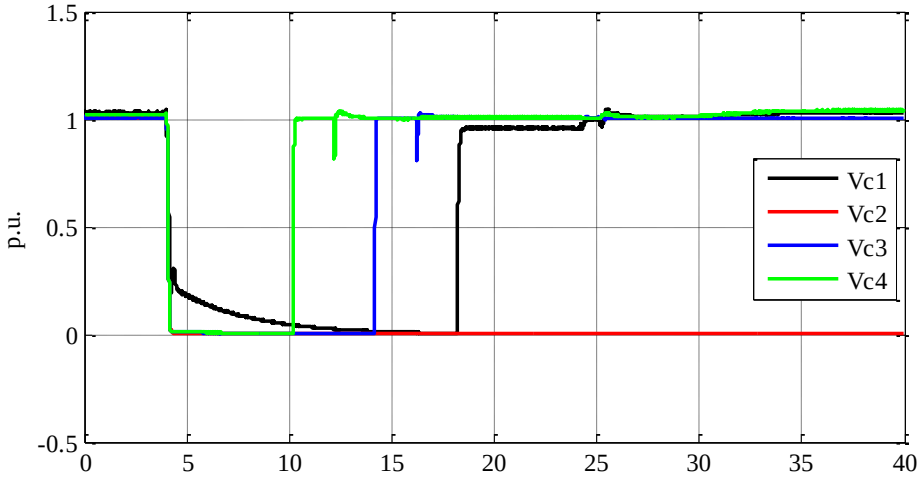
The fault is applied at 4 s on DC Cable 2 as a permanent pole-to-pole fault. The system performance using the proposed control and protection sequence in Section 6.3.4 is demonstrated in Figure 6-18: (a) DC voltages of the MTDC; (b) DC currents of the MTDC; (c) MMC AC-side voltages in RMS value; (d) MMC AC-side currents in RMS value; (e) active power; (f) reactive power.



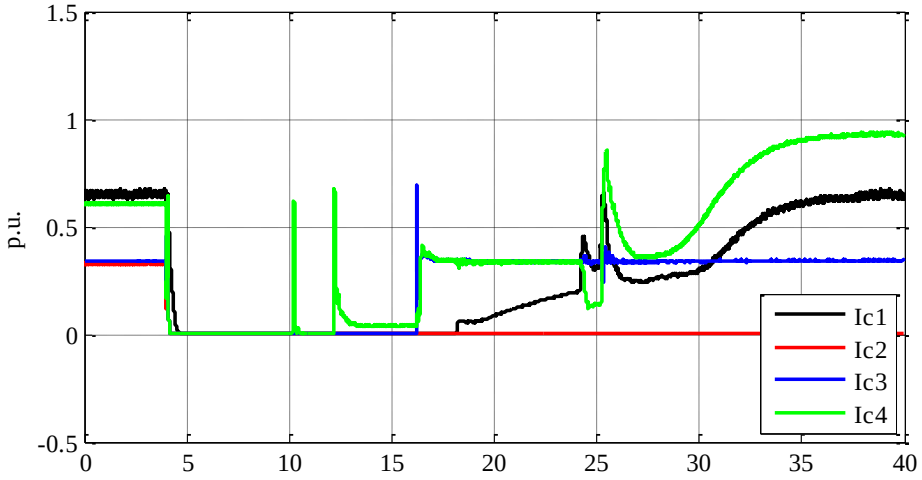
(a)


Idc1
Idc2
Idc3
Idc4
p.u.
Time (s)

(b)


Vc1
Vc2
Vc3
Vc4
p.u.
Time (s)

(c)


Ic1
Ic2
Ic3
Ic4
p.u.
Time (s)

(d)

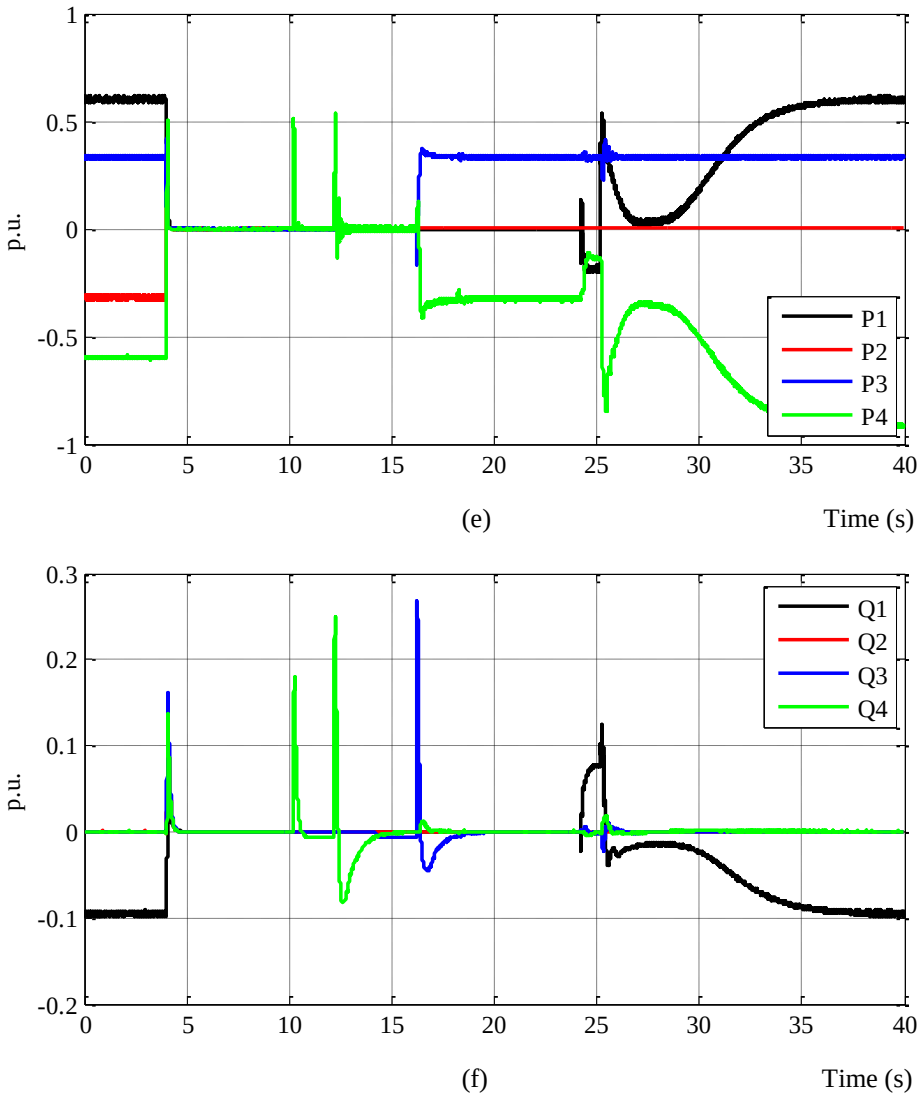


Figure 6-18 System performance under an DC fault on DC Cable 2 using proposed control and protection sequence

Figure 6-18(a) demonstrates that DC voltages drop to around 0.25 p.u. after the fault isolation. According to Table 6-4, the system recovery control starts at 8.17 s and the control mode of T4 is switched to DC voltage control. At 10.17 s, T4 resumes and then establishes the DC voltage of the MTDC, which is well stabilised afterwards. Figure 6-18(b) shows that current surges emerge at the MMC DC-side after the fault, but they soon decrease due to effective fault isolation operation. During the system recovery stage, the unfaulted terminals resume smoothly with small current surges. Figure 6-18(c) shows that due to effective fault isolation,

MMC AC-side voltages decrease gradually with no significant oscillations. During the system recovery phase, T4, T3, T2 resume nominal operating condition in sequence. Figure 6-18(d) shows that no overcurrent emerges at MMC AC-side with the fault isolation strategy. During the system recovery phase, AC-sides of MMC-4, MMC-3, MMC-2 resume stable current transfer in sequence. Figure 6-18(e) demonstrates that due to effective control and protection strategy, the active power of the MTDC decreases to 0 after the fault with almost no oscillations. During the system recovery stage, T4, T3, T2 resume normal power transfer in sequence. Figure 6-18(f) shows small oscillations of reactive power during the whole process.

The simulation results justify the proposed control and protection sequence, which achieves: effective fault isolation and faulted section isolation, effective adjustment of the control mode of T4 to realise stable and smooth resume of the unfaulted terminals.

6.3.5.2 Case B

In order to present the control and protection sequence for the MTDC system with coordinated droop control under the same DC fault and the corresponding system performance, in this case, the MTDC system applies droop control rather than master-slave control. Due to the fact that droop control mode includes information of both the active power and the DC voltage, and will adjust the reference of active power depending on the change of the measured DC voltage, the terminals with droop control have the ability to support DC voltage. Therefore, the switching of control mode is not necessary and is avoided at the system recovery phase. In this case, MMC-1 uses the original constant AC voltage control, while voltage droop is used by MMC-2, MMC-3 and MMC-4.

When the same DC fault occurs at T2, the control and protection sequence is proposed in

Figure 6-19. Table 6-5 describes the control action at each instant and the delay between 2 sequential actions.

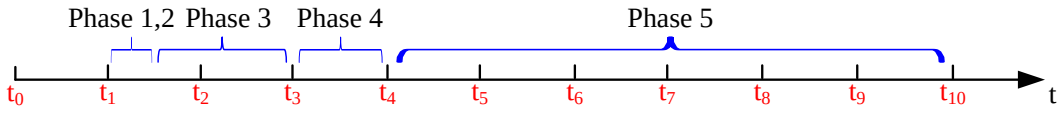


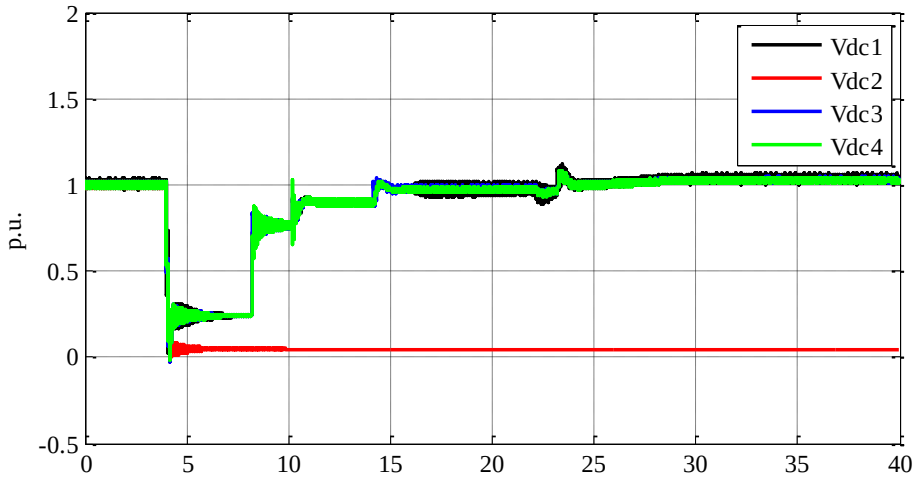
Figure 6-19 Control and protection sequence under DC fault on DC Cable 2 with the MTDC using voltage droop control

Table 6-5 Description of the Control and Protection Sequence in Figure 6-19

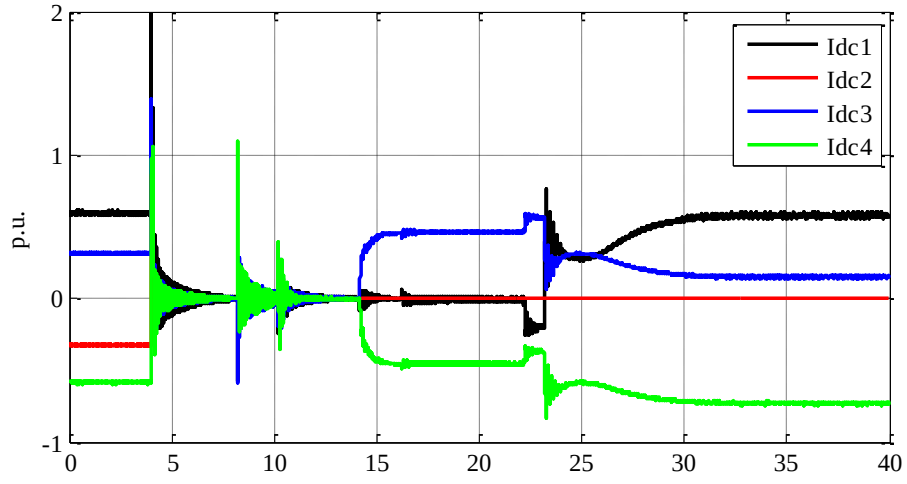
t_n	Time	Description	Comment
t_0	0 s	System under normal operation	
t_1	4 s	Apply the DC fault on DC Cable 2	
t_2	4.002 s	Block all MMCs	An MMC can be blocked as fast as 2-5 ms;
t_3	4.08 s	Trip all AC *CBs* and *CBW*, block the OWF	An AC CB can generally be tripped within 60-100 ms;
t_4	4.2 s	Open *ISW2*	A DC *ISW* can be opened when its current becomes sufficiently small;
t_5	8.2 s	Reclose *CB3*	A delay of 2 s is set between two sequential control actions. This delay can be shortened as long as the system reaches a steady condition after the former control action.
t_6	10.2 s	Deblock MMC-3	
t_7	12.2 s	Reclose *CB4*	
t_8	14.2 s	Deblock MMC-4	
t_9	16.2 s	Deblock MMC-1	
t_{10}	22.2 s	Reclose *CBW*	The re-integration of the OWF needs a stable AC voltage at *PCC1*. Hence, a long delay of 6 s is chosen.
t_{11}	23.2 s	Deblock the *OWF*	

It can be seen that the resume of the unfaulted terminals starts at 8.2 s by directly resuming T3 without switching control mode of any terminal in prior. The system state after the resume of the unfaulted terminals is the same as Figure 6-17.

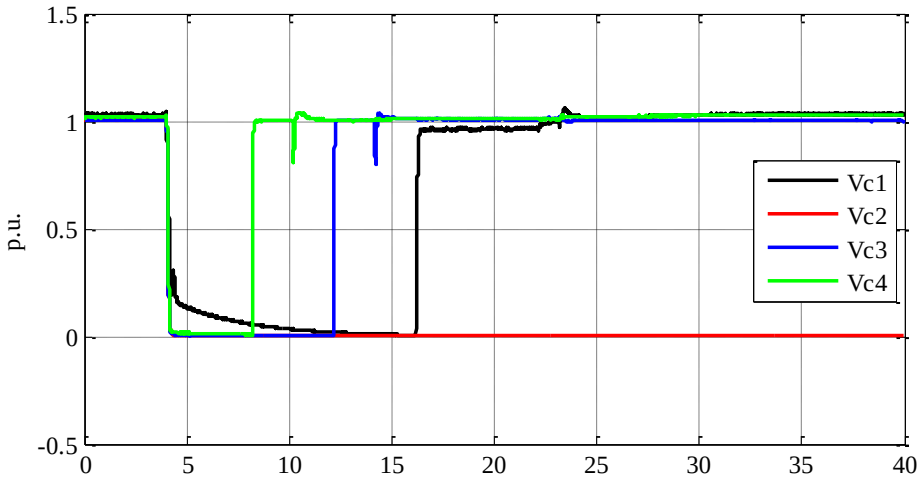
A real-time simulation is conducted on the RTDS using the control and protection sequence in Figure 6-19 and the system performance is demonstrated in Figure 6-20: (a) DC voltages of the MTDC; (b) DC currents of the MTDC; (c) MMC AC-side voltages in RMS value; (d) MMC AC-side currents in RMS value; (e) active power; (f) reactive power.



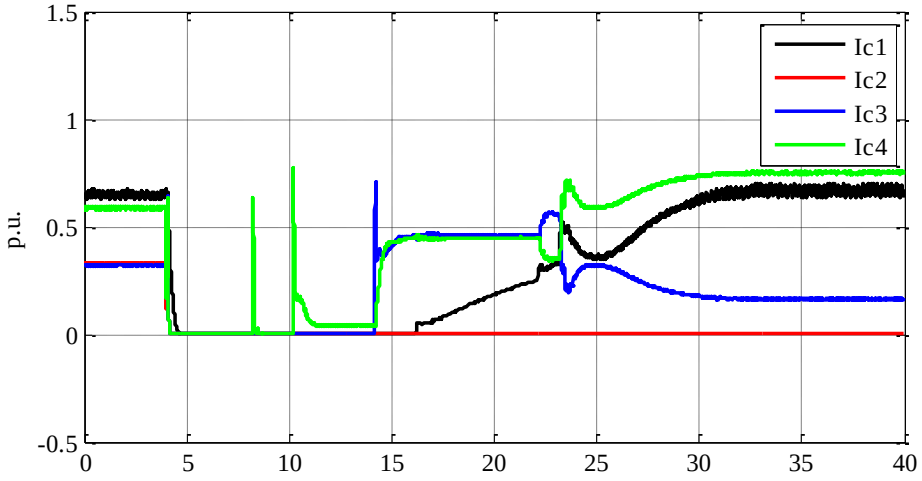
(a)



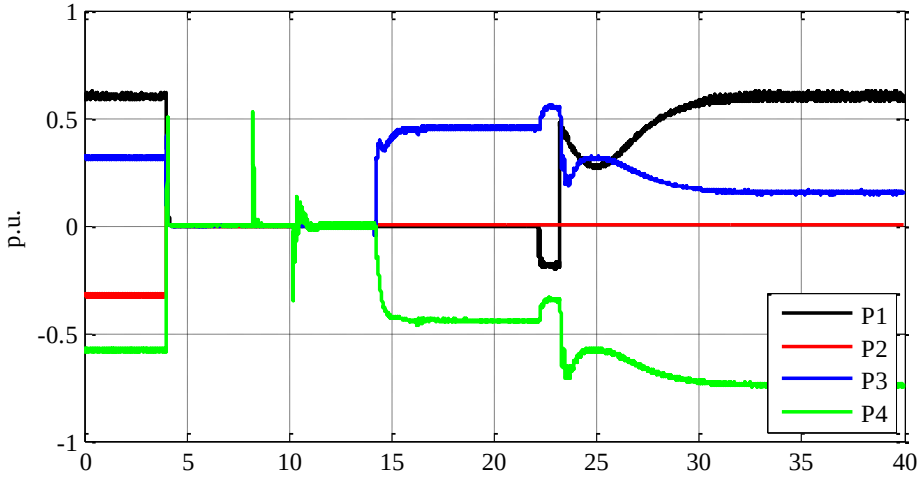
(b)


1.5
1
0.5
0
-0.5
p.u.
0
5
10
15
20
25
30
35
40
Vc1
Vc2
Vc3
Vc4
Time (s)

(c)


1.5
1
0.5
0
-0.5
p.u.
0
5
10
15
20
25
30
35
40
Ic1
Ic2
Ic3
Ic4
Time (s)

(d)


1
0.5
0
-0.5
-1
p.u.
0
5
10
15
20
25
30
35
40
P1
P2
P3
P4
Time (s)

(e)

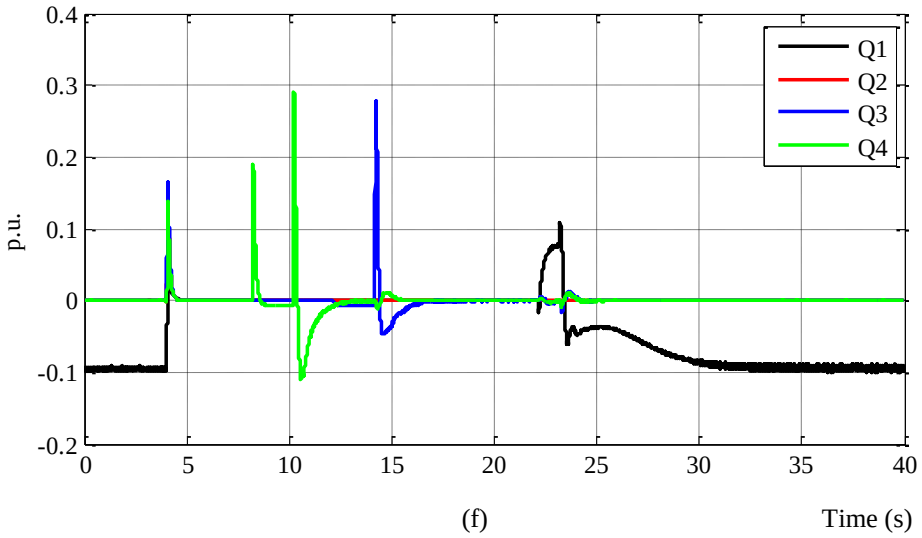


Figure 6-20 System performance with droop control mode under an DC fault on DC Cable 2 using proposed control and protection sequence

It can be seen that with the addition of droop control, the resume of the unfaulted terminals and the reconfiguration of the MTDC system is achieved and become simpler without the need of switching control mode. However, the control and protection sequence used here cannot be applied for the MTDC system with master-slave control. The test system uses master-slave control and the control and protection sequence becomes complex when a fault occurs at the master terminal, but the control and protection sequence can be regarded as a feasible and back-up solution, which has a wide range of applicability. Nevertheless, both control and protection sequences proposed could be beneficial for practical engineering.

Considering the fact that the MTDC system with master-slave control may have the potential risk of having complex process of control and protection, such as switching of control mode, under fault conditions at the master terminal, it is suggested that both AC-side and DC-side of the master terminal has strong networks with low rate of fault. Otherwise, the coordinated droop control is more favourable in MTDC applications.

6.4 Summary

In this chapter, control and protection against a permanent DC pole-to-pole fault has been investigated. 2 different fault conditions: one is that the fault occurs at one slave terminal, while the other one is that the fault occurs at the master terminal, have been investigated respectively. For the fault occurring at one of the slave terminals, the control and protection strategy at the phase of fault isolation and faulted section isolation has been proposed according to the system fault characteristics. After the faulted section isolation, 3 main issues have been discussed for the control and protection strategy at the system recovery phase. They are: 1) when to start the resume of the unfaulted terminals; 2) for each of the unfaulted terminals, what is the control sequence between deblocking of the MMC and reclosing of the AC circuit breaker; 3) for the MTDC system, what is the recovery sequence of each terminal. The solution of them have been proposed as: 1) the resume of the unfaulted terminals will start when all DC currents on the DC grid have completely decayed to 0; 2) for the terminal with an active AC network, the AC circuit breaker is reclosed prior to the deblocking of the MMC; for the terminal with a passive AC network, the MMC is deblocked prior to the reclosing of the AC circuit breakers; 3) the terminals with active AC networks resume prior to the terminal with a passive AC network; for the terminals with active AC networks, the master terminal resumes prior to the slave terminals. Based on these solutions, a practical DARC scheme for the system recovery control has been proposed. Combining the DARC scheme and the control and protection strategy at the phases of fault isolation and faulted section isolation, a comprehensive control and protection sequence has been proposed. The effectiveness of the proposed control and protection sequence has been proved by real-time simulations. The discussion and case studies were conducted taking the fault occurring at T1 as example. Since T1, T3, T4 are all slave terminals regulating the active power, the proposed

control and protection sequence can be similarly applied.

For the fault occurring at the master terminal, similarly, according to the system fault characteristics, the control and protection strategy for the fault isolation and faulted section isolation has been proposed. It has been found that the control and protection strategy at these phases is similar to that for the former fault condition. However, the control and protection strategy at the system recovery phase is different, since the master terminal cannot resume due to the fault location, leading to the absence on the DC voltage control. In order to resume the unfaulted terminals, one of the terminals with active power control needs to switch control mode to take over the DC voltage control. Combining the former DARC scheme, a modified DARC scheme has been proposed for the system recovery under the DC fault at the master terminal. A comprehensive control and protection sequence has been formed and verified by real-time simulation results.

Due to the fact that the introduction of the coordinated droop control can avoid the switching of control mode during the system recovery phase, the control and protection strategy has been discussed with detailed control and protection sequence proposed. A simulation case study has proved its effectiveness. It has been observed that the control and protection sequence becomes simpler thanks to the use of voltage droop control. In addition, if ac AC fault occurs at the AC-side of MMC-2, which was discussed in Section 5.3, the fault can be isolated without interrupting the adjacent terminals with the use of droop control. However, the control and protection strategy for the MTDC with droop control cannot fully be applied for the MTDC system with master-slave control. The proposed control and protection for the MTDC system with master-slave control can be regarded as a feasible and back-up solution, which has a wide application range, which may be valuable for industrial applications.

Nevertheless, master-slave control is more suitable for the MTDC system which has a strong master terminal with low failure rates such as cable model. Otherwise, droop control has more advantages and is more favourable in the MTDC applications.

CHAPTER 7 CONCLUSIONS AND FUTURE WORK

As the final chapter of this thesis, conclusions of the main work and research outcomes are presented. Based on the work that has been accomplished, future work that deserves further research and study is suggested.

7.1 Conclusions

Due to environmental concerns and the potential shortage of conventional energy, the development of renewable energy has drawn more and more attention. In the utilisation of renewable energy, wind energy, especially offshore wind energy, has attracted much interest and occupies a large proportion of future renewable schemes. For the integration of offshore wind energy, the use of the current state-of-the-art, MMC HVDC technology, including MMC MTDC technology, has advantages. The innovations and breakthroughs on the VSC-based power electronic devices, which enhance the system rating and efficiency and lower the costs, further promote the development of this technique.

This thesis has conducted comprehensive investigations on an offshore integrated MMC MTDC system. The main work of the thesis can be concluded as follows:

1. The system performance under the steady-state condition and transient conditions has been studied. Under steady-state condition, the system operating condition has been calculated, providing the nominal values of the voltages, currents, active and reactive power. According to the calculated operating condition, an assumption has been given for the operating requirement for the system under transient conditions, which provides the corresponding control objectives. The system performance between two steady-states,

including the change of wind speed and wind intermittency, ramping of power at one terminal and power flow reversal, has been demonstrated. The test system has presented the adaptability to wind swinging. The capability of the power balancing and power reversal of the MTDC have been evaluated. In addition, the established system on the RTDS has shown its controllability and observability.

2. The start-up control of the system has been investigated. According to the characteristics of the AC networks that connect with the MTDC, the system terminals have been categorised into the onshore terminals with active AC networks and the offshore terminal with the OWF, which is regarded as a passive AC network before start-up. For the MMCs at the onshore terminals, the operating characteristics during the start-up process have been analysed. The second-order mathematical models have been derived before and after the deblocking of the MMC. According to the analysis of the mathematical models, a hierarchical start-up control scheme has been proposed for the MMCs with active AC networks. For the offshore MMC, since the MMC cannot be pre-charged from the OWF side before the start-up of the OWF, the pre-charging of the MMC is executed from the DC side. The second-order mathematical models have been derived before and after the deblocking of the MMC. According to the analysis of the mathematical models, a start-up scheme with reduced DC voltage has been proposed for the MMC with a passive AC network. By combining the hierarchical start-up control scheme and the reduced DC voltage start-up control scheme, a sequential start-up control scheme has been formed for the start-up control of the MTDC system. This scheme could effectively start the MTDC system with minimum voltage difference on the SM capacitors when deblocking the MMCs. Based on the proposed start-up control scheme, a comprehensive start-up control sequence has been proposed and evaluated by real-time simulations. In comparison to the other two start-up control schemes, the

superiority of the proposed scheme on mitigating the voltage spikes and current surges has been observed. Some features of using the proposed start-up control scheme have been concluded:

- Since each terminal is started in sequence instead of starting the terminals randomly or starting all terminals simultaneously, the system is started in a stable manner;
- Appropriate adjustment of the controlled DC voltage is important and can minimise the voltage difference on the SM capacitors when deblocking the MMC, which contributes to small voltage spikes and current surges;
- Appropriate settings of the AC voltage and active power can reduce the possibility of the emergence of the overvoltages and overcurrents during the start-up process.

The investigated start-up control is meaningful for the self-start-up of the MTDC system without external devices and could be useful for practical engineering.

3. The control and protection strategy for the MTDC system under the MMC-side AC fault has been investigated. Since the fault occurs beyond the protection range of the nearby AC circuit breakers and is permanent, the associated control and protection strategy applied will be different to the traditional control and protection strategy.

For the fault at one of the slave terminals, the system fault characteristics have been analysed and have indicated the necessity for prompt control and protection actions to physically isolate the fault. The associated control and protection strategy at the fault isolation phase has been proposed. Since the implementation of the fault isolation does not affect or interrupt the operation of the unfaulted terminals, there is no control action needed for the system recovery. For the fault at the master terminal with DC voltage control, control and protection strategy at

the fault isolation phase has been proposed according to the analysis of the fault characteristics. Since the implementation of the fault isolation has an impact on and interrupts the operation of the unfaulted terminals, the control and protection strategy for the system recovery needs to be considered. Due to the fact that the fault occurs at the master terminal and is permanent, the master terminal will not resume after the fault isolation. Hence, one of the unfaulted terminals has to switch its control mode to take over the DC voltage control and the remaining unfaulted terminals will resume afterwards. For both cases, comprehensive control and protection sequences have been proposed and justified by RTDS simulations.

Previous proposals for control and protection against AC faults were predominantly established under the assumption that the faulted-side MMC can be blocked successfully, which is not always necessarily valid. This thesis has investigated different conditions of blocking failure on the faulted-side MMC after the fault occurs. It includes: 1) the MMC completely fails to be blocked; 2) one converter arm completely fails to be blocked; 3) one converter arm partly fails to be blocked. According to the analysis and simulation results, 1) and 2) have been categorised into emergency condition, necessitating a special control and protection action to isolate the fault. A special control and protection strategy, which can effectively isolate the fault and faulted section, has been proposed and evaluated by real-time simulations. 3) has been considered to be the non-emergency condition in which the special control and protection action is not required. However, if the number of successfully blocked SMs is less than half of the SMs on the converter arm, a potential risk that the successfully blocked SMs may experience being overcharged has been identified.

The research on the AC fault conditions, especially some severe conditions such as the fault inside the converter station and the blocking failure of the MMC, has highlighted the potential

problems that may exist in the development of future MTDC systems and has proposed corresponding solutions which could be utilised as a feasible and back-up scheme for the control and protection system.

4. Control and protection against permanent DC fault conditions using the traditional protection scheme with AC circuit breakers has been investigated. The research focus has been mainly put on the system recovery control of the MTDC after the fault isolation.

For the DC fault occurring at one slave terminal, the fault isolation and faulted section isolation strategy have been proposed according to the fault characteristics. During the system recovery phase, 3 important issues have been discussed: 1) when to start the recovery control; 2) for each terminal, what is the control sequence between the deblocking of the MMC and reclosing of the AC circuit breakers; 3) for the MTDC, what is the recovery sequence of each terminal. The solutions have been proposed that: 1) the recovery control is started when all the DC currents in the MTDC have completely decayed to 0; 2) for the terminal with active AC networks, the AC circuit breaker is reclosed prior to the deblocking of the MMC; for the terminal with a passive AC network, the MMC is deblocked prior to the reclosing of the AC circuit breaker; 3) the terminals with active AC networks resume prior to the recovery of the terminal with a passive AC network; for the terminals with active AC networks, the master terminal resumes prior to the slave terminals. Based on the solutions, a practical DARC scheme has been proposed for the system recovery control. Combining the DARC scheme with the control and protection strategy at the fault isolation phase, a comprehensive control and protection sequence has been proposed and verified by RTDS simulations. The superiority of the proposed control and protection sequence has been observed in comparison with the control and protection sequence with a different recovery control scheme.

For the DC fault occurring at the master terminal, the control and protection strategy at the fault isolation and faulted section isolation phase has been proposed and is similar to that of the former fault condition. However, the control and protection strategy at the system recovery phase is different, since the master terminal cannot resume, leading to the absence on the DC voltage control. A modified DARC scheme has been proposed for the system recovery by switching the control mode of one of the unfaulted terminals to DC voltage control and then resumes the unfaulted terminals. This thesis has also discussed the MTDC with coordinated voltage droop control which can avoid the switching of control mode during the system recovery phase. Comprehensive control and protection sequences have been proposed for the MTDC with master-slave control and voltage droop control, respectively, and the system performance has been evaluated by RTDS simulations. It has been concluded that although the recovery control of the MTDC with master-slave control is more complex under the DC fault at the master terminal, the proposed control and protection strategy is a feasible solution which has a wide application range and may be beneficial for practical engineering. Nevertheless, master-slave control is more suitable for the MTDC system which has a strong master terminal with low failure rates. Otherwise, voltage droop control may be more favourable in the MTDC applications in which the system can resume in a more efficient and simpler manner under DC fault conditions.

7.2 Future Work

For offshore integrated MMC MTDC systems, there are still many issues that deserve further investigation. On the basis of the research of this thesis, the following aspects are suggested for further exploitation:

1. For the start-up control investigated in Chapter 4,

- The time interval between two sequential control actions can be further optimised, so as to complete the start-up process of the MTDC in a more efficient manner.
- The start-up control of the MTDC uses a self-start-up approach. It would be meaningful to investigate the start-up control using a hybrid approach which combines both the self-start-up and external voltage sources approaches, to determine whether the zero voltage difference on SMs can be achieved when deblocking the MMCs.
- Master-slave control is applied in the MTDC, the impact of coordinated voltage droop control on the start-up control performance deserves investigation.
- The MTDC has 4 terminals which are in radial topology. The impact of the complexity of the topology of the MTDC and the increased number of terminals on the start-up control performance deserves further investigation.

2. For the control and protection strategy against AC fault conditions in Chapter 5,

- It would be interesting to investigate whether some DC current components may flow from the DC-side into the faulted AC-side, which may stop the AC circuit breaker from being normally tripped under different conditions, such as different configurations of the AC transformers or different fault locations.
- The proposed control and protection sequence can be further optimised, such as reduce the time interval between two sequential control actions or combine some actions at the same instant, to achieve the system recovery in a more efficient manner.
- When an AC fault occurs at the AC-side of MMC-1, since V_{ac}-f control does not have a current limiter, the fault current from the MMC AC-side cannot be limited. It would be interesting to explore an alternative approach to limit the current, such as add

another interface component to function as the current limiter.

3. For the control and protection against DC fault conditions in Chapter 6,

- The proposed control and protection sequence can be further optimised to resume the system in a more efficient manner.
- When there are a higher number of terminals such as in the Cigre full DC grid testing system with 16 converter terminals, the effective and appropriate control and protection strategy deserves investigation.
- It would be interesting to compare the advanced protection techniques, such as hybrid DC circuit breakers, DC-DC converters, full-bridge MMC, and the traditional protection technique, in terms of different aspects: 1) the time needed to isolate the fault; 2) the complexity of the control and protection strategy; 3) the losses; 4) the cost.
- It would be valuable to investigate the use of hybrid control and protection techniques, so as to achieve the optimal cost effective scheme.

4. Some other topics:

- Different with traditional energy sources, renewable energy sources have intermittent characteristics and cannot provide sufficient inertia to the power system. Hence, the stability of the power system may be largely impacted with the increased amount of renewable generation integration and replacement of traditional energy sources. How to effectively stabilise the power system, e.g. increasing the installation of ESS, interconnection of different areas using MTDC, will be an important research topic and a technical challenge.
- An ESS has a maximum energy storage capacity and may be able to provide either

transient support of large amount of power or long-term support of small amount of power according to the specific conditions and the control objectives. Hence, the amount of ESS that is suitable for integration into an MTDC system and the effective control of ESS to implement different functions to support the MTDC system under various conditions deserves investigation.

- The design of the system model and the control of the MMC have a large impact on the system performance. Hence, the comparison of the system performance under various conditions between the current model in which the converter is 7-level half-bridge MMC and the other models in which the MMC has higher levels deserves investigation.
- When the MTDC has over 3 terminals, while the topology is in a meshed topology, effective control of the power flow on each DC branch deserves investigation.
- The design of the power flow controller for meshed MTDC grids and its control system deserves investigation.
- The control performance and the ability of blocking DC fault current of the power flow controller deserve investigation.

APPENDIX A

A.1 Configuration of the MTDC Test System

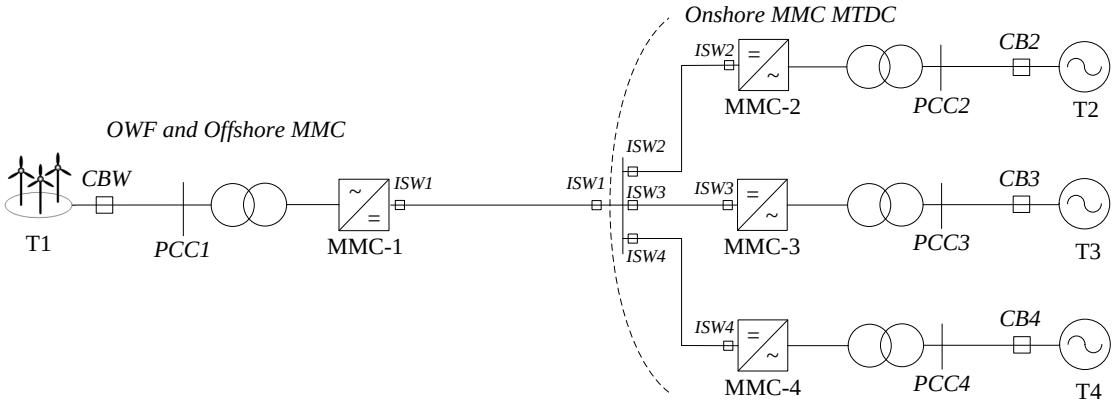


Figure A-1 Configuration of the OWF integrated 4-terminal MMC HVDC system

This is a 4-terminal MMC HVDC system where the OWF is integrated at T1. *Tn* (*n* = 1,…,4) denotes each terminal of the MTDC system; *CBW* denotes the AC circuit breaker at the OWF terminal; *CBn* (*n* = 1,…,4) denotes the AC circuit breaker at each terminal; *PCCn* (*n* = 1,…,4) denotes the point of common coupling at each terminal; MMC-*n* (*n* = 1,…,4) denotes the MMC at each terminal; DC *ISWn* (*n* = 1,…,4) denotes the DC isolation switch at each terminal.

A.2 Measuring Points of the System in the Simulations

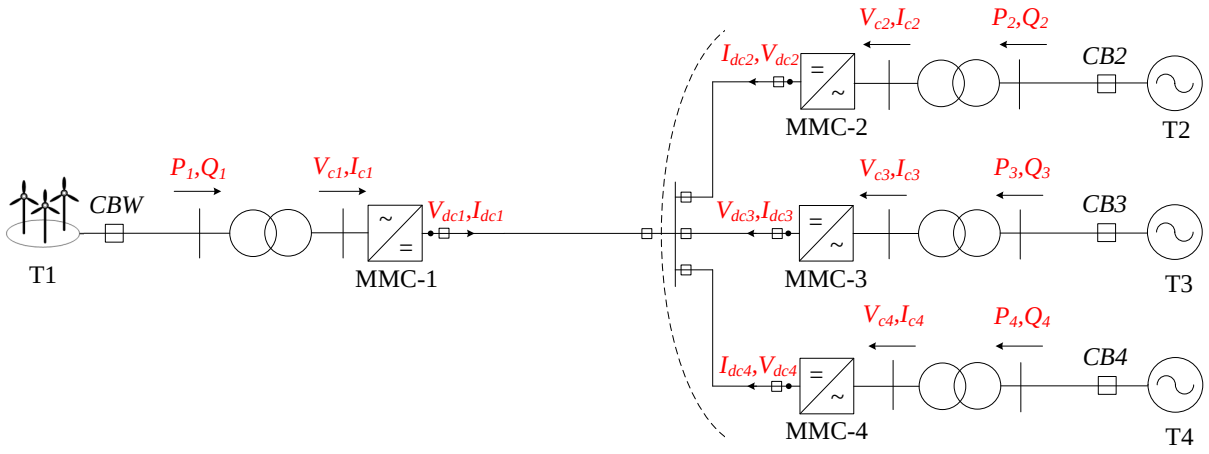


Figure A-2 Measuring points of the MTDC

The measuring points in the simulations are illustrated in Figure A-2. P_n and Q_n (n = 1,…,4) denote the active power and reactive power measured at the PCC; V_{cn} and I_{cn} (n = 1,…,4) denote the MMC AC-side voltage and current measured in RMS value; V_{dcn} and I_{dcn} (n = 1,…,4) denote the DC voltage and current measured at each terminal.

A.3 Parameters of the MTDC Test System

Table A-1 Parameters of the MTDC Test System

Parameters	Values	Comments
AC system voltage	138 kV	L-N, RMS
AC system inductance L_{AC}	150 mH	SCR = 8 at PCC
Transformer ratio	138 kV/30 kV	Y/Δ
Transformer leakage inductance	5%	
Wind turbine rated output	1.4 MW	
No. of wind turbines	60	
Wind farm rated output	84 MW	
DC bus voltage $V_{dc}/2$	50 kV	± 50 kV
MMC rating	150 MVA	
No. of SMs per arm	6	
Arm inductance L_a	3 mH	
SM capacitance C	2500 μF	
Diode resistance R_d	0.02 Ω	
T3 active power P_3^*	50 MW	Import to MTDC
T4 active power P_4^*	90 MW	Export from MTDC
Reactive power reference	0 MVar	T2, T3, T4

APPENDIX B

B.1 MMC Models in the RTDS

There are two main models for MMC modelling, average model and detailed switching model, in the RTDS library.

B.1.1 Average Model of MMC

Figure B-1 present one converter arm of an MMC using the average model.

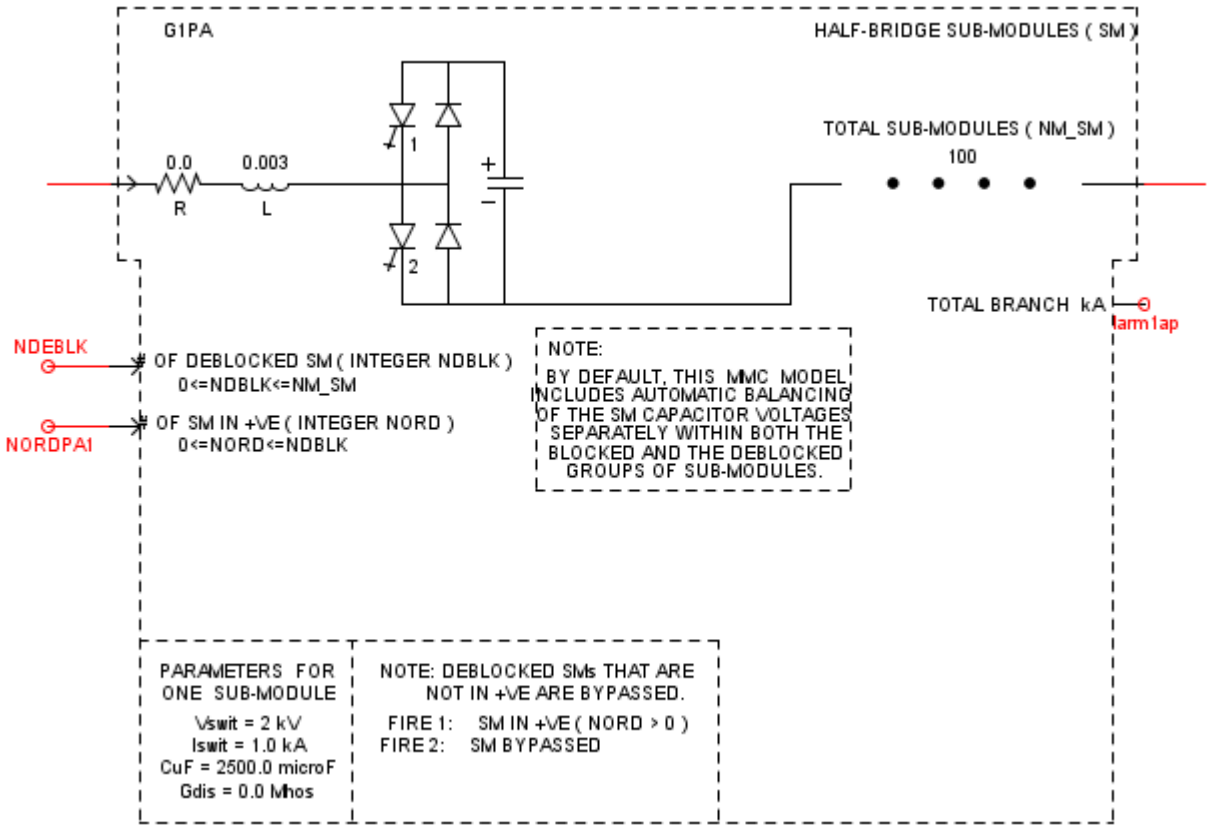


Figure B-1 Average model of the MMC in the RTDS library – MMC4

The average model, namely MMC4 in the RTDS library, can simulate up to 640 SMs per

converter arm. The capacitor voltage balancing is not necessary and it is assumed that the capacitor voltages of all SMs are always the same in this model. Hence, the internal dynamics of the MMC, i.e. charging and discharging of each individual SM capacitor are not explicitly simulated. However, the external dynamics of the MMC, i.e. the MMC AC- and DC-side voltages and currents, are well presented. In addition, the computational requirement of this model is much lower than that of the detailed switching model. Hence, this model is suitable for the analysis and simulation of the performance of MTDC networks with many converters using MMC topologies, while the internal characteristics of the MMCs are not the main research focus.

B.1.2 Detailed Switching Model of MMC

Figure B-2 present one converter arm of an MMC using the detailed switching model.

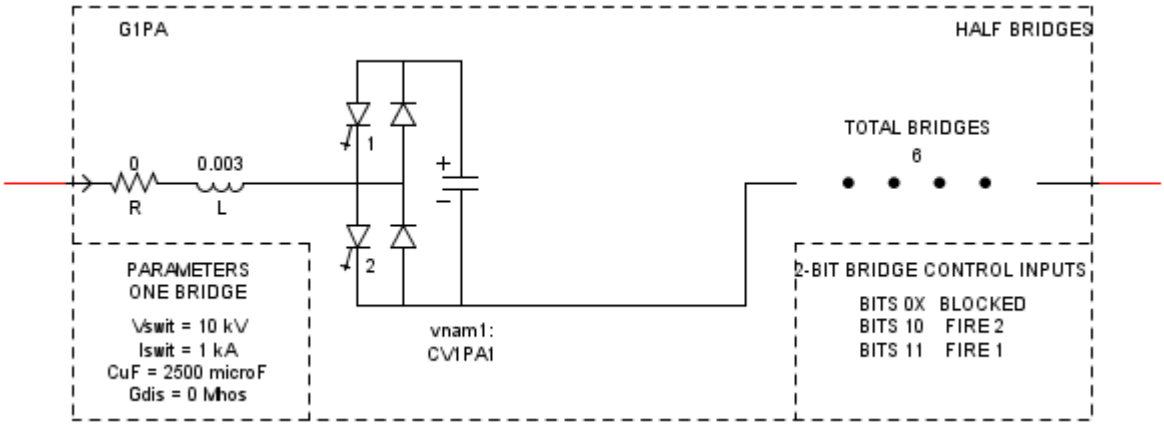


Figure B-2 Detailed switching model of the MMC in the RTDS library – MMC ChainV3

The detailed switching model, namely MMC ChainV3 in the RTDS library, can simulate up to 56 SMs per converter arm. The capacitor voltage balancing control is required and the capacitor voltage of each SM can be monitored in real-time. Hence, the internal dynamics of the MMC, i.e. charging and discharging of each individual SM capacitor are explicitly

represented. However, the computational burden of this model becomes a challenge, which requires model processors to be used in the simulation. Considering the computation requirement and allocation of processors, the RTDS simulation with MMC ChainV3 is generally up to 16 SMs per converter arm. Hence, this model is suitable for the analysis and simulation of the internal characteristics of the MMC or the performance of MTDC networks with limited number of converters using MMC topologies.

RTDS Company has recently developed new models for the modelling of MMC. For the average model, there are currently two models, MMC4 and MMC5, which can be used. For the detailed switching model, MMC ChainV3 and MMC ChainV5 can be used. In addition, an FPGA-based MMC model, namely MMC U5 model, can be used for detailed modelling up to 512 SMs per converter arm. More information about the details of these models can be found in [149]-[150].

B.2 Mathematical Representation of MMC

This section presents a mathematical representation of MMC through the analysis of one phase of the converter as shown in Figure B-3 [131], [151].

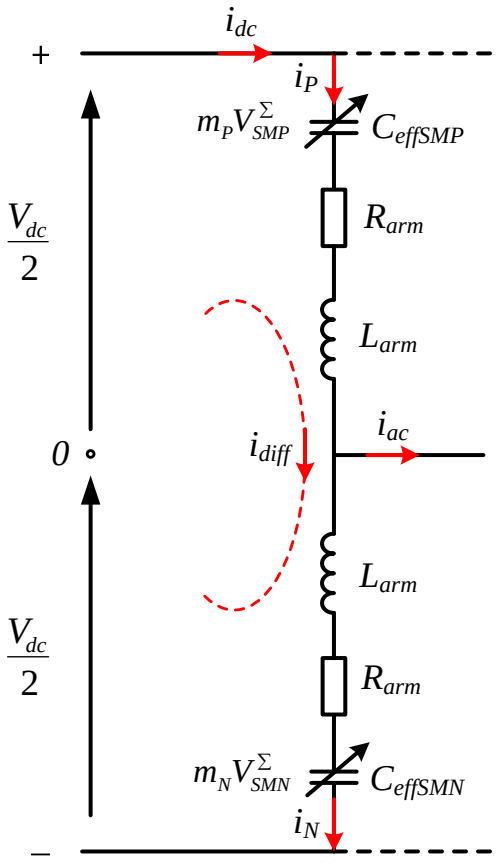


Figure B-3 Modelling of one phase of MMC [131], [151]

In Figure B-3, L_{arm} represents the MMC arm inductance; the total power losses on the converter arm are represented by an equivalent resistance R_{arm}; C_{effSMi} (i = P, N) represents the effective inserted capacitance. Since the control of MMC is achieved by regulating the number of inserted/bypassed, an MMC arm can be regarded as an equivalent circuit with series connected resistance, inductance and variable capacitance.

If the sum of the SM capacitor voltages is V_{SMi}^{Σ} (i = P, N), the effective inserted capacitor voltage $V_{effSMi}(t)$ can be represented as:

$$V_{effSMi}(t) = m_i(t) \cdot V_{SMi}^{\Sigma} \tag{B.1}$$

where $m_i(t)$ is the modulation index of the inserted capacitors.

Since the total number of SMs on one converter arm is *N*, the number of effective inserted capacitors is $m_i(t) \cdot N$. If the capacitance of one SM is C_{SM}, the capacitance of effective inserted capacitors can be calculated as:

$$C_{effSMi} = \frac{C_{SM}}{m_i(t) \cdot N} \tag{B.2}$$

For the average model of MMC, it is assumed that the SM capacitor voltages are well balanced and total SM capacitors are represented by one effective inserted capacitor. When the arm current $i_i(t)$ flows through the effective inserted capacitor, the dynamics of total SM capacitors can be described as:

$$\frac{dV_{SMi}^{\Sigma}}{dt} = \frac{i_i(t)}{C_{effSMi}} \tag{B.3}$$

Substituting C_{effSMi} in (B.2) into (B.3), we have

$$\frac{dV_{SMi}^{\Sigma}}{dt} = \frac{Nm_i(t)}{C_{SM}} \cdot i_i(t) \tag{B.4}$$

For the upper arm, we have

$$\frac{dV_{SMP}^{\Sigma}}{dt} = \frac{Nm_P(t)}{C_{SM}} \cdot i_P(t) \tag{B.5}$$

For the lower arm, we have

$$\frac{dV_{SMN}^{\Sigma}}{dt} = \frac{Nm_N(t)}{C_{SM}} \cdot i_N(t) \tag{B.6}$$

According to the current direction references shown in Figure B-3, the following relationship can be derived based on KCL:

$$i_P - i_N = i_{ac} \tag{B.7}$$

The relationship between the inner difference current i_{diff} and the MMC AC-side current is:

$$i_P = i_{diff} + \frac{i_{ac}}{2} \tag{B.8}$$

$$i_N = i_{diff} - \frac{i_{ac}}{2} \tag{B.9}$$

Hence, the inner difference current can be expressed as:

$$i_{diff} = \frac{i_P + i_N}{2} \tag{B.10}$$

Considering the upper and lower converter arm and based on KVL, we have

$$v_c = \frac{V_{dc}}{2} - R_{arm} \cdot i_P - L_{arm} \frac{di_P}{dt} - m_P V_{SMP}^{\Sigma} \tag{B.11}$$

$$v_c = -\frac{V_{dc}}{2} + R_{arm} \cdot i_N + L_{arm} \frac{di_N}{dt} + m_N V_{SMN}^{\Sigma} \tag{B.12}$$

Subtracting (B.12) from (B.11), we have:

$$0 = V_{dc} - 2R_{arm} \cdot i_{diff} - 2L_{arm} \frac{di_{diff}}{dt} - \left(m_P V_{SMP}^{\Sigma} + m_N V_{SMN}^{\Sigma}\right)$$

$$\frac{di_{diff}}{dt} = -\frac{R_{arm}}{L_{arm}} \cdot i_{diff} - \frac{m_P}{2L_{arm}} \cdot V_{SMP}^{\Sigma} - \frac{m_N}{2L_{arm}} \cdot V_{SMN}^{\Sigma} + \frac{V_{dc}}{2L_{arm}} \tag{B.13}$$

Substituting (B.8) into (B.5) and (B.9) into (B.6), we have

$$\frac{dV_{SMP}^{\Sigma}}{dt} = \frac{Nm_P(t)}{C_{SM}} \cdot i_{diff} + \frac{Nm_P(t)}{C_{SM}} \cdot \frac{i_{ac}}{2} \tag{B.14}$$

$$\frac{dV_{SMN}^{\Sigma}}{dt} = \frac{Nm_N(t)}{C_{SM}} \cdot i_{diff} - \frac{Nm_N(t)}{C_{SM}} \cdot \frac{i_{ac}}{2} \tag{B.15}$$

Therefore, according to (B.13), (B.14), and (B.15), the system differential equations can be obtained as follows [131], [151]:

$$\frac{d}{dt}\begin{bmatrix} i_{diff} \\ V_{SMP}^{\Sigma} \\ V_{SMN}^{\Sigma} \end{bmatrix} = \begin{bmatrix} -\frac{R_{arm}}{L_{arm}} & -\frac{m_P}{2L_{arm}} & -\frac{m_N}{2L_{arm}} \\ \frac{Nm_P}{C_{SM}} & 0 & 0 \\ \frac{Nm_N}{C_{SM}} & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{diff} \\ V_{SMP}^{\Sigma} \\ V_{SMN}^{\Sigma} \end{bmatrix} + \begin{bmatrix} \frac{V_{dc}}{2L_{arm}} \\ \frac{Nm_P i_{ac}}{2C_{SM}} \\ -\frac{Nm_N i_{ac}}{2C_{SM}} \end{bmatrix} \tag{B.16}$$

For the detailed switching model of MMC, the SM capacitor voltages are not automatically balanced and capacitor voltage balancing control is necessary, i.e. only the effective inserted SM capacitors are charged/discharged by the arm current and the associated capacitor voltages will increase/decrease, while the remaining SM capacitors are bypassed and the associated capacitor voltages will remain unchanged. Since only the effective inserted capacitor voltages are impacted, in the detailed switching model of MMC, (B.3) will be modified as:

$$\frac{dV_{effSMi}}{dt} = \frac{i_i(t)}{C_{effSMi}} \tag{B.3'}$$

The system differential equations in (B.13), (B.14), and (B.15) are modified as:

$$\frac{di_{diff}}{dt} = -\frac{R_{arm}}{L_{arm}} \cdot i_{diff} - \frac{1}{2L_{arm}} \cdot V_{effSMP} - \frac{1}{2L_{arm}} \cdot V_{effSMN} + \frac{V_{dc}}{2L_{arm}} \tag{B.13'}$$

$$\frac{dV_{effSMP}}{dt} = \frac{Nm_P(t)}{C_{SM}} \cdot i_{diff} + \frac{Nm_P(t)}{C_{SM}} \cdot \frac{i_{ac}}{2} \tag{B.14'}$$

$$\frac{dV_{effSMN}}{dt} = \frac{Nm_N(t)}{C_{SM}} \cdot i_{diff} - \frac{Nm_N(t)}{C_{SM}} \cdot \frac{i_{ac}}{2} \tag{B.15'}$$

Therefore, according to (B.13'), (B.14'), and (B.15'), the system differential equations for the detailed switching model of MMC can be obtained as follows:

$$\frac{d}{dt}\begin{bmatrix} i_{diff} \\ V_{effSMP} \\ V_{effSMN} \end{bmatrix} = \begin{bmatrix} -\frac{R_{arm}}{L_{arm}} & -\frac{1}{2L_{arm}} & -\frac{1}{2L_{arm}} \\ \frac{Nm_P}{C_{SM}} & 0 & 0 \\ \frac{Nm_N}{C_{SM}} & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{diff} \\ V_{effSMP} \\ V_{effSMN} \end{bmatrix} + \begin{bmatrix} \frac{V_{dc}}{2L_{arm}} \\ \frac{Nm_P i_{ac}}{2C_{SM}} \\ -\frac{Nm_N i_{ac}}{2C_{SM}} \end{bmatrix} \tag{B.16'}$$

APPENDIX C

C. Mechanical Model for Wind Turbine

The mechanical model for the wind turbine is combined with the DFIG and the Multimass model. The Multimass computes the speed of its masses through the integration of the difference between the electrical torque and mechanical torque. The mechanical power output of the wind turbine under steady-state is derived based on [126], [152]–[153] and is expressed as:

$$P_m = c_p(\lambda,\beta)\frac{\rho A}{2}v_{wind}^3 \tag{C.1}$$

where P_m is the mechanical power output of the wind turbine; $c_p(\lambda,\beta)$ is the performance coefficient, which is a function of the tip speed ratio λ and the blade pitch angle β; ρ is the air density; A is the area swept out by the turbine blade; v_{wind} is the wind velocity.

The performance coefficient, c_p, is used to evaluate the efficiency of the wind turbine of converting the wind energy to the mechanical energy. According to literature [152], [154], the following two equations are selected to describe the dynamics of the performance coefficient:

$$c_p(\lambda,\beta) = \left[(C_1 - C_2\beta)\sin\left[1.5707\frac{(\lambda - 3y(\lambda))}{(C_3 - C_4\beta)}\right] - (\lambda - 3y(\lambda))C_5\beta\right] + \frac{C_6}{(1+\lambda)} \tag{C.2}$$

where

$$y(\lambda) = \left(1.0 - e^{-\frac{\lambda}{3}} \right) \tag{C.3}$$

and

$$c_p(\lambda, \beta) = C_1 \left[\frac{C_2}{\lambda_1} - C_3\beta - C_4 \right] e^{-\frac{C_5}{\lambda_i}} + C_6\lambda \tag{C.4}$$

where

$$\frac{1}{\lambda_i} = \frac{1}{\lambda + 0.08\beta} - \frac{0.035}{\beta^3 + 1} \tag{C.5}$$

The tip speed ratio λ is defined as:

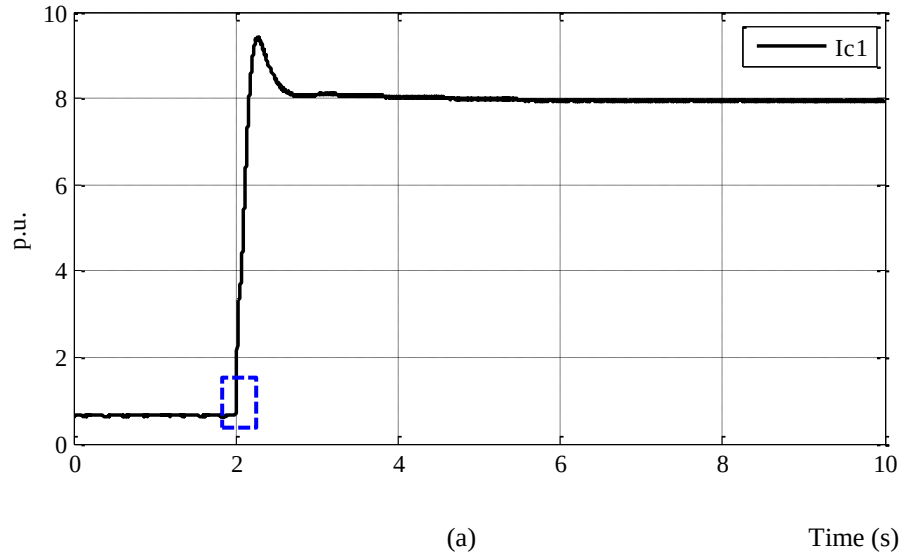
$$\lambda = \frac{R\omega}{v_{wind}} \tag{C.6}$$

where R is the turbine radius; ω is the rotational speed of the turbine.

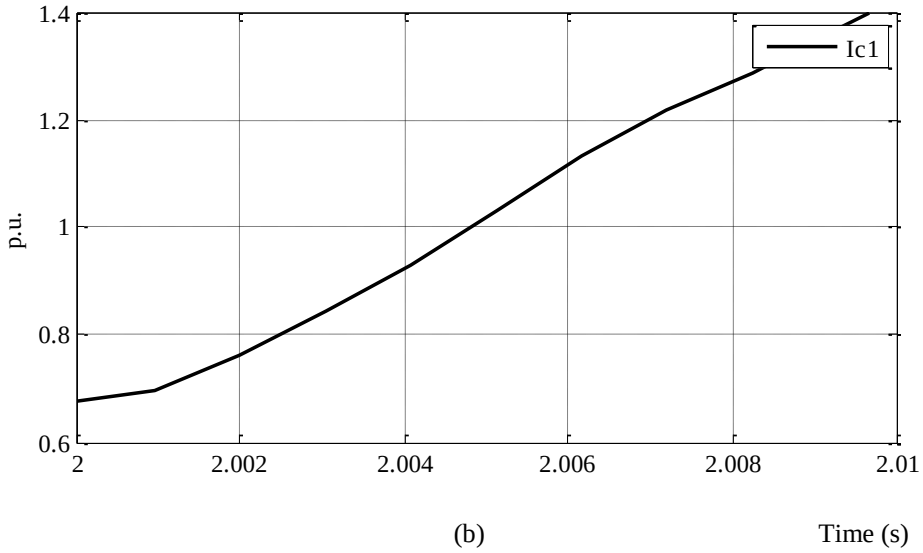
APPENDIX D

D. Calculation of Fault Current

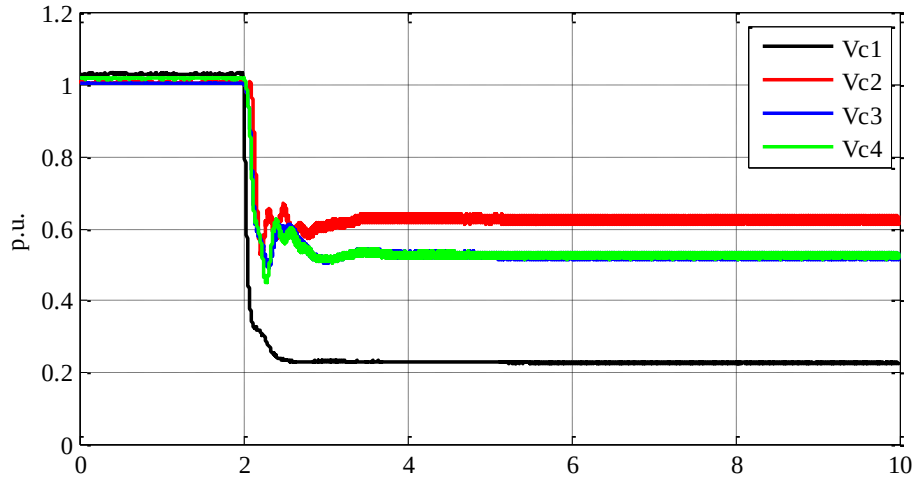
The system performance under the three-phase to ground permanent AC fault at 2 s with MMC-1 complete blocking failure is demonstrated in Figure D-1: (a) MMC-1 AC-side current in RMS value; (b) zoomed proportion of (a); (c) MMC-1 AC-side voltage in RMS value; (d) zoomed proportion of (c).



(a)



(b)



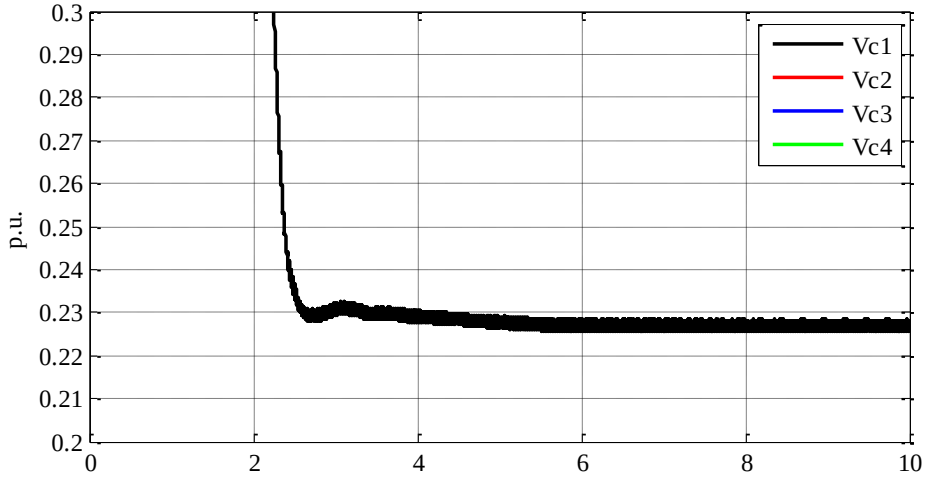


Figure D-1 System Performance under MMC-1 AC-side fault with MMC-1 complete blocking failure using the basic control and protection sequence

Figure D-1(a) and (c) demonstrates that MMC-1 AC-side RMS current finally stabilises at around 8 p.u. and MMC-1 AC-side RMS voltage finally stabilises at around 0.227 p.u. The simulated earth fault resistance is 0.5 Ω. Hence, we have $V_{c,L-L,RMS} = 0.227$ p.u., $I_{c,L-L,RMS} = 8$ p.u., and $R_f = 0.5\ \Omega$

The base values of the MMC-1 AC-side voltage and current are

$V_{base} = 51.96 \text{ kV},\ I_{base} = 1.6667 \text{ kA}$

The actual value of MMC-1 AC-side voltage can be calculated as:

$$V_{a,L-L,RMS} = V_{c,L-L,RMS} \cdot V_{base} = 0.227 * 51.96 = 11.8 \text{ kV}$$

The peak value of the line-to-neutral voltage at MMC-1 AC-side is

$$V_{a,L-N,peak} = V_{a,L-L,RMS} \cdot \frac{\sqrt{2}}{\sqrt{3}} = 11.8 * \frac{\sqrt{2}}{\sqrt{3}} = 9.63 \text{ kV}$$

The peak value of the current at MMC-1 AC-side is

$$I_{a,L,peak} = \frac{V_{a,L-N,RMS}}{R_f} = \frac{9.63}{0.5} = 19.26 \text{ kA}$$

The RMS value of the current at MMC-1 AC-side can be calculated as

$$I_{a,L,RMS} = I_{a,L,peak} \cdot \frac{1}{\sqrt{2}} = 19.26 * \frac{1}{\sqrt{2}} = 13.62 \text{ kA}$$

The per unit value of the MMC-1 AC-side RMS current is

$$I_{c,L,RMS} = \frac{I_{a,L,RMS}}{I_{base}} = \frac{13.62}{1.6667} = 8.172 \text{ p.u.}$$

The calculation result of MMC-1 AC-side RMS current is around 8 p.u., which meets the simulation result in the RTDS. The small error is due to the fact that the calculation is based on ideal condition without considering the disturbance factors, such as the harmonics. Therefore, the RTDS simulation result of the fault current is justified by the calculation.

PUBLICATIONS AND OUTCOMES

During the PhD study, the following articles have been published/submitted:

International Journal Publications

[1] P. Wang, X. P. Zhang, P. F. Coventry, and R. Zhang, "Start-up control of an offshore integrated MMC multi-terminal HVDC system with reduced DC voltage," *IEEE Transactions on Power Systems*, DOI: 10.1109/TPWRS.2015.2466600 (accepted for publication).

[2] P. Wang, X. P. Zhang, P. F. Coventry and Z. Li, "Control and protection strategy for MMC MTDC system under converter-side AC fault during converter blocking failure," *Journal of Modern Power Systems and Clean Energy*, vol. 2, no. 3, pp. 272–281, Sept. 2014.

[3] N. Deng, P. Wang, X. P. Zhang, G. Tang and J. Cao, "A DC current flow controller for meshed modular multilevel converter multiterminal HVDC grids," *CSEE Journal of Power and Energy Systems*, vol. 1, no. 1, pp. 43–51, Mar. 2015.

[4] P. Wang, X. P. Zhang, R. Zhang, P. F. Coventry and Z. Li, "Control and protection sequence for recovery and reconfiguration of an offshore integrated MMC multi-terminal HVDC system under DC faults," *International Journal of Electrical Power & Energy Systems*, (submitted and currently under review).

[5] N. Deng, P. Wang, and X. P. Zhang, "Small signal stability analysis and control system design of a meshed multi-terminal HVDC grid with a current flow controller," *Electric Power Components and Systems*, (submitted and currently under revision).

[6] N. Deng, P. Wang, and X. P. Zhang, "A multi-line current flow controller with droop control in meshed DC grids," *IET Generation, Transmission and Distribution*, (under preparation).

International Conference Publications

[7] P. Wang, X. P. Zhang, N. Deng, P. F. Coventry and R. Zhang, "Control and

protection sequence of an offshore integrated MMC MTDC system with master-slave/droop control under converter AC-side fault," in *6th International Conference on Advanced Power System Automation and Protection (APAP 2015)*, Sept. 2015, pp. 1–5.

[8] P. Wang, Z. Li, X. P. Zhang, R. Zhang and P. F. Coventry, "DC fault management for VSC MTDC system using delayed-auto-re-configuration scheme," in *11th IET International Conference on AC/DC Power Transmission*, Feb. 2015, pp. 1–7.

[9] P. Wang, Z. Li, X. P. Zhang and P. F. Coventry, "Start-up sequences of an offshore integrated MMC MTDC system," in *11th IET International Conference on AC/DC Power Transmission*, Feb. 2015, pp. 1–7.

[10] N. Deng, X. P. Zhang, P. Wang, X. Gu, and M. Wu, "A converter-based general interface for AC microgrid integrating to the grid," in *4th IEEE Innovative Smart Grid Technologies Europe (ISGT Europe)*, Oct. 2013, pp. 1–5.

[11] R. Shi, X. P. Zhang, D.C. Kong, N. Deng and P. Wang, "Dynamic impacts of fast-charging stations for electric vehicles on active distribution networks," in *IEEE Innovative Smart Grid Technologies Asia (ISGT Asia)*, Apr. 2012, pp. 1–6.

Apart from the above publications, the author has contributed to the following report:

[12] "Simulation of multi-terminal VSC HVDC system by means of real time digital simulator (RTDS)," Project Report for National Grid, Dec. 2013.

LIST OF REFERENCES

[1] V. F. Lescale, “Modern HVDC: state of the art and development trends,” in *Int. Conf. on Power System Technology (POWERCON '98)*, Aug. 1998, pp. 446–450.

[2] Compendium of all HVDC projects, Cigre SC B4, 2009.

[3] K. Meah and S. Ula, “Comparative evaluation of HVDC and HVAC transmission systems,” in *Proc. Power Eng. Soc. General Meeting*, Jun. 2007, pp. 1–5.

[4] M. P. Bahrman and B. K. Johnson, “The ABCs of HVDC transmission technologies,” *IEEE Power Energy Magazine*, vol. 5, no. 2, pp. 32–44, Mar./Apr. 2007.

[5] E. Selvaraj, C. P. Sugumaran, Krishnamoorthi, M. Kumar, M. R. Joshi, J. Ganesan, S. Geethadevi, and S. Kumar, “A review on fundamentals of HVDC transmission,” *J. Club for Electrical Engineering (JCEE)*, vol. 1, no. 1, pp. 1–7, Sept. 2014.

[6] B. Anderson and C. D. Barker, “A new era in HVDC?,” *Inst. Elect. Eng. Rev.*, vol. 46, no. 2, pp. 33–39, Mar. 2000.

[7] N. Flourentzou, V. Agelidis, and G. Demetriades, “VSC-based HVDC power transmission systems: An overview,” *IEEE Trans. Power Electron.*, vol. 24, no. 3, pp. 592–602, Mar. 2009.

[8] D. Van Hertem and M. Ghandhari, “Multi-terminal VSC HVDC for the European supergrid: Obstacles,” *Renew. Sustain. Energy Rev.*, vol. 14, no. 9, pp. 3156–3163, Dec. 2010.

[9] U. Axelsson, A. Holm, C. Liljegren, M. Aberg, K. Eriksson, and O. Tollerz, “The Gotland HVDC Light Project—Experiences from trial and commercial operation,” in *CIRED Conf.*, 2001, pp. 1–5.

[10] S. P. Teeuwsen, “Modeling the Trans Bay Cable Project as voltage-sourced converter with modular multilevel converter design,” in *IEEE Power Energy Soc. General Meeting*, Jul. 2011, pp. 1–8.

[11] G. Asplund, K. Eriksson, and K. Svensson, “HVDC light—DC transmission based on voltage-sourced converters,” *ABB Rev.*, vol. 1, pp. 4–9, 1998.

[12] R. Marquardt, “Stromrichterschaltungen mit verteilten Energiespeichern,” German Patent, DE10103031A1, Jan. 24, 2001.

[13] T. C. Green, M. M. C. Merlin, N. Okaeme, and D. R. Trainer, “Modular multilevel converter,” Patent WO 2012/055435 A1, May 3, 2012.

[14] G. Tang, Z. He, and H. Pang, “R&D and application of voltage source converter based high voltage direct current engineering technology in China,” *J. Mod. Power Syst. Clean Energy*, vol. 2, no. 1, pp. 1–15, Mar. 2014.

[15] J. Rodriguez, J.-S. Lai, and F. Z. Peng, “Multilevel inverters: a survey of topologies, controls, and applications,” *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Aug. 2002.

[16] C. Oates and C. Davidson, “A comparison of two methods of estimating losses in the modular multi-level converter,” in *Proc. Eur. Conf. Power Electron. Appl.*, 2011, pp. 1–10.

[17] A. M. Gole and R. Wachal, “Voltage source converter (VSC) IET tutorial,” in *Proc. 10th IET Int. Conf. AC/DC Power Transmission*, Dec. 2012.

[18] P. S. Jones and C. Davidson, “Calculation of power losses for MMC-based VSC HVDC stations,” in *15th Euro. Conf. Power Electron. Appl. (EPE)*, pp.1–10, France, September 2013.

[19] N. Ahmed, S. Norrga, H.-P. Nee, A. Haider, D. V. Hertem, L. Zhang, L. Harnefors, “HVDC SuperGrids with modular multilevel converters — The power transmission backbone of the future,” in *9th Int. Multi-Conf. Syst. Signals Devices (SSD)*, pp. 1–7, Mar. 2012.

[20] T. Modeer, H. P. Nee, and S. Norrga, “Loss comparison of different sub-module implementations for modular multilevel converters in HVDC applications,” in *Proc. 14th Eur. Power Electron. Appl. Conf.*, pp. 1–7, Sept. 2011.

[21] C. C. Davidson and D. R. Trainer, “Innovative concepts for hybrid multilevel converters for HVDC power transmission,” in *Proc. 9th IET Int. Conf. AC/DC Power Transmission*, Oct. 2010, pp. 1–5.

[22] M. Davies, M. Dommaschk, J. Dorn, J. Lang, D. Retzmann, D. Soerangr, “HVDC PLUS – basics and principle of operation”, Siemens Tech. Rep., 2008.

[23] Å. M. H. Kjørholt, “HVDC transmission using a bipolar configuration composed of an LCC and MMC,” Master dissertation, Norwegian University of Science and Technology, Trondheim, Norway, 2014.

[24] P. F. Coventry, “Implementing innovation in the grid – multi-terminal VSC HVDC links,” in *Proc. 10th IET Int. Conf. AC/DC Power Transmission*, Dec. 2012.

[25] G. P. Adam, O. Anaya-Lara, and G. Burt, “Multi-terminal DC transmission system based on modular multilevel converter,” in *Proc. 44th Int. Universities Power Eng. Conf.*, Sept. 2009, pp. 1–5.

[26] D. Woodford, “Symmetrical monopole VSC transmission,” *Electranix Technical Paper,* Mar. 2014.

[27] Adam G. P. and Williams B. W., "Half- and full-bridge modular multilevel converter models for simulations of full-scale HVDC links and multiterminal DC grids," *IEEE J. Emerging and Selected Topics in Power Electron.*, vol. 2, no. 4, pp. 1089–1108, 2014.

[28] R. Marquardt, “Modular multilevel converter: An universal concept for HVDC-networks and extended dc-bus-applications,” in *Proc. Int. Power Electron. Conf.*, Jun. 2010, pp. 502–507.

[29] R. Marquardt, “Modular multilevel converter topologies with dc-short circuit current limitation,” in *Proc. IEEE 8th Int. Power Electron. ECCE Asia Conf.*, Jun. 2011, pp. 1425–1431.

[30] Z. Xu, Y. Xue, and Z. Zhang, “VSC-HVDC technology suitable for bulk power overhead line transmission,” *Proc. of CSEE*, vol. 34, no. 29, pp. 5051–5062, Oct. 2014 (in Chinese).

[31] M. Merlin, T. Green, P. Mitcheson, D. Trainer, R. Critchley, W. Crookes, and F. Hassan, “The alternate arm converter: A new hybrid multilevel converter with dc-fault blocking capability,” *IEEE Trans. Power Del.*, vol. 29, no. 1, pp. 310–317, Feb. 2014.

[32] Y. Xue, Z. Xu, and Q. Tu, “Modulation and control for a new hybrid cascaded multilevel converter with dc blocking capability,” *IEEE Trans. Power Del.*, vol. 27, no. 4, pp. 2227–2237, Oct. 2012.

[33] T. M. Haileselassie, “Control, dynamics and operation of multi-terminal VSC-HVDC transmission systems,” Ph.D. dissertation, Norwegian University of Science and Technology, Trondheim, Norway, 2012.

[34] X.-P. Zhang, “Multiterminal Voltage-Sourced Converter Based HVDC Models for Power Flow Analysis,” *IEEE Trans. Power Syst.*, vol. 18, no. 4, pp. 1877–1884, Nov. 2004.

[35] X.-P. Zhang, R. Zhang, P. F. Coventry, “Fault management of the MT VSC HVDC using delayed auto-re-configuration (DARC) schemes”, Project Report For National Grid, Jun. 2011.

[36] C. D. Barker and R. S. Whitehouse, “A current flow controller for use in HVDC grids, ” in *Proc. 10th IET Int. Conf. AC/DC Power Transmission*, Dec. 2012, pp. 1–5.

[37] D. Jovcic and B.-T. Ooi, “Developing DC transmission networks using DC transformers,” *IEEE Trans. Power Del.*, vol. 25, no. 4, pp. 2535–2543, Oct. 2010.

[38] T. M. Haileselassie and K. Uhlen, “Power system security in a meshed north sea HVDC grid,” *Proc. IEEE*, vol. 101, no. 4, pp. 978–990, Feb. 2013.

[39] N. R. Chaudhuri and B. Chaudhuri, “Adaptive droop control for effective power sharing in multi-terminal DC (MTDC) grids,” *IEEE Trans. Power Syst.*, vol. 28, no. 1, pp. 21–29, Feb. 2013.

[40] W. Wang and M. Barnes, “Power flow algorithms for multi-terminal VSC-HVDC with droop control,” *IEEE Trans. Power Syst.*, vol. 29, no. 4, pp. 1721–1730, Jul. 2014.

[41] C. Dierckxsens, K. Srivastava, M. Reza, S. Cole, J. Beerten, and R. Belmans, “A distributed DC voltage control method for VSC MTDC systems,” *Elect. Power Syst. Res.*, vol. 82, no. 1, pp. 54–58, Jan. 2012.

[42] G. Nakou, “In depth renewable energy – Analysis – A 2020 vision for UK energy,” *IET Eng. & Tech.*, vol. 2, no. 7, pp. 18–19, Jul. 2007.

[43] "UK renewable energy roadmap," Department of Energy & Climate Change (DECC) Report, Jul. 2011.

[44] X.-P. Zhang and P. Zeng, "Marine energy technology," *Proc. IEEE*, vol. 101, no. 4, pp. 862–865, 2013.

[45] E. M. Robertson, A. D. Alarcon-Rodriguez, S. J. Galloway, and W. Ault Graham, "Outline for an integrated multiple energy carrier model of the UK energy infrastructure," in *Proc. 44th Int. Universities Power Eng. Conf. (UPEC)*, Sept. 2009, pp. 1–5.

[46] H. Forster, S. Healy, C.Loreck and F. Matthes, "Analysis of the EU's energy roadmap 2050 scenarios," Smart Energy for Europe Platform, 2012.

[47] J. C. Garcia and F. Mosallat, "Wind integration through HVDC-VSC links," Workshop Presentation, in *IET 11th Int. Conf. AC/DC Power Transmission*, Feb. 2015.

[48] R. Ulsund, "Offshore power transmission – Submarine high voltage transmission alternatives", Master dissertation, Norwegian University of Science and Technology, Trondheim, Norway, 2009.

[49] N. M. Kirby, L. Xu, M. Luckett, and W. Siepmann, "HVDC transmission for large offshore wind farms," *IEE Power Eng. J.*, vol. 16, no. 3, pp. 135–141, Jun. 2002.

[50] *PSS/E-29 Program Application Guide: Volume I,* Siemens PTI Ltd, 2002.

[51] *PSCAD user's guide: Version 4.2.1,* Manitoba HVDC Research Centre, 2010.

[52] U. N. Gnanarathna, A. M. Gole, and R. P. Jayasinghe, "Efficient modeling of modular multilevel HVDC converters (MMC) on electromagnetic transient simulation programs," *IEEE Trans. Power Del.*, vol. 26, no. 1, pp. 316–324, Jan. 2011.

[53] J. Peralta, H. Saad, S. Dennetiere, J. Mahseredjian, and S. Nguefeu, "Detailed and averaged models for a 401-Level MMC-HVDC system," *IEEE Trans. Power Del.*, vol. 27, no. 3, pp. 1501–1508, Jul. 2012.

[54] HVDC grid feasibility study, CIGRÉ Working Group B4–52 Rep. no. 533, Apr. 2013.

[55] H. Saad, J. Peralta, S. Dennetiere, J. Mahseredjian, J. Jatskevich, J. A. Martinez, A. Davoudi, M. Saeedifard, V. Sood, X. Wang, J. Cano, and A. Mehrizi-Sani, "Dynamic

averaged and simplified models for MMC-based HVDC transmission systems.," *IEEE Trans. Power Del.*, vol. 28, no. 3, pp. 1723–1730, Jul. 2013.

[56] F. B. Ajaei and R. Iravani, "Enhanced equivalent model of the modular multilevel converter," *IEEE Trans. Power Del.*, vol. 30, no. 2, pp. 666–673, Apr. 2015.

[57] J. Xu, A. M. Gole, and C. Zhao, "The use of averaged-value model of modular multilevel converter in DC grid," *IEEE Trans. Power Del.*, vol. 30, no. 2, pp. 519–528, Apr. 2015.

[58] B. Wang, X. Dong, Z. Bo, A. Klimek, B. Caunce, A. Perks, B. Smith, and L. Denning, "RTDS environment development of ultra-high-voltage power system and relay protection test," in *Proc. Power Energy Soc. Gen. Meet.*, Jun. 2007, pp. 1–7.

[59] X. Lin, K. Ou, Y. Zhang, H. Guo, and Y. Chen, "Simulation and analysis of the operating characteristics of MMC based VSC-MTDC system," in *4th IEEE PES Innovative Smart Grid Tech. (ISGT) Europe*, Oct. 2013, pp. 1–5.

[60] K. Ou, H. Guo, X. Liu, Z., and L. Guan, "The research of the control strategies for 4-terminal VSC-HVDC system based on multi point voltage control and their implement," in *China Int. Conf. Elect. Distrib. (CICED)*, Sept. 2014, pp. 748–753.

[61] K. Ou, H. Rao, Z. Cai, H. Guo, X. Lin, L. Guan, T. Maguire, B. Warkentin, and Y. Chen, "MMC-HVDC simulation and testing based on real-time digital simulator and physical control system," *IEEE J. Emerging and Selected Topics in Power Electron.*, vol. 2, no. 4, pp. 1109–1116, Dec. 2014.

[62] S. Elimban, Y. Zhang, "Real time simulation for HVDC grids with modular multi-level converters," in *Proc. IET 11th Int. Conf. AC/DC Power Transmission*, Feb. 2015.

[63] H. Duchen, M. Lagerkvist, R. Kuffel, R. Wierckx, "HVDC simulation and control testing using a real-time digital simulator (RTDS)," in *1st Int. Conf. Digital Power Syst. Simulators (ICDS)*, Apr. 1995, pp. 213–218.

[64] L. Han, Y. Han, Z. Wang, M. Claus, D. Retzmann, and D. Povh, "Verification of HVDC controller using an advanced hybrid real-time simulator," in *Int. Conf. Power Syst. Tech.*, China, Aug. 1998, pp. 493–497.

[65] B. Wang, X. Dong, Z. Bo, and A. Perks, "RTDS environment development of ultra-high-voltage power system and relay protection test," *IEEE Trans. Power Del.*, vol. 23, no. 2, pp. 618–623, Apr. 2008.

[66] S. Arunprasanth, U. D. Annakkage, C. Karawita and R. Kuffel, "A generic point-to-point MMC-VSC system for real-time and off-line simulation studies," in *Int. Conf. Power Syst. Transients (IPST)*, Croatia, pp. 1–7, Jun. 2015.

[67] *RTDS official website: PSS/E & MATLAB/Simulink Integration*, RTDS Technologies, available online at https://www.rtds.com/the-simulator/our-software/psse-and-matlab-integration/.

[68] C. Schauder and H. Mehta, "Vector analysis and control of advanced static VAr compensators," *IEE Proc. C Gen. Trans. Distrib.*, vol. 140, pp. 299–306, Jul. 1993.

[69] I. Papic, P. Zunko, D. Povh, and M. Weinhold, "Basic control of unified power flow controller," *IEEE Trans. Power Syst.*, vol. 12, pp. 1734–1739, Nov. 1997.

[70] L. Xu, L. Yao, and C. Sasse, "Grid integration of large DFIG-based wind farms using VSC transmission," *IEEE Trans. Power Syst.*, vol. 22, no. 3, pp. 976-984, Aug. 2007.

[71] M. Saeedifard and R. Iravani, "Dynamic performance of a modular multilevel back-to-back HVDC system," *IEEE Trans. Power Del.*, vol. 25, no. 4, pp. 2903–2912, Oct. 2010.

[72] J. Cao, W. Du, H. F. Wang, and S. Q. Bu, "Minimization of transmission loss in meshed AC/DC grids with VSC-MTDC networks," *IEEE Trans. Power Syst.*, vol. 28, no. 3, pp. 3047–3055, Aug. 2013.

[73] N. Yousefpoor, S. Kim, and S. Bhattacharya, "Multi-terminal DC grid control under loss of terminal station," in *IEEE Energy Conv. Cong. Exposition (ECCE)*, Sept. 2014, pp. 744–749.

[74] T. M. Haileselassie and K. Uhlen, "Impact of DC line voltage drops on power flow of MTDC using droop control," *IEEE Trans. Power Syst.*, vol. 27, no. 3, pp. 1441–1449, Aug. 2012.

[75] C. D. Barker, R. S. Whitehouse, S. Wang, and J. Liang, "UK risk of multiple cross-over of control characteristics in multiterminal HVDC," in *Proc. IET 11th Int. Conf. AC/DC Power Transmission*, Feb. 2015.

[76] J. Qin and M. Saeedifard, "Reduced switching-frequency voltage balancing strategies for modular multilevel HVDC converters," *IEEE Trans. Power Del.*, vol. 28, no. 4, pp. 2403–2410, Oct. 2013.

[77] Q. Tu, Z. Xu, and L. Xu, "Reduced switching-frequency modulation and circulating current suppression for modular multilevel converters," *IEEE Trans. Power Del.*, vol. 26, no. 3, pp. 2009–2017, Jul. 2011.

[78] M. Guan, Z. Xu, and H. Chen, "Control and modulation strategies for modular multilevel converter based HVDC System," in *Proc. Conf. IEEE Ind. Electron. Soc.*, 2011, pp. 849–854.

[79] S. Debnath, J. Qin, B. Bahrani, M. Saeedifard, and P. Barbosa, "Operation, control, applications of the modular multilevel converter: A review," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 37–53, Jan. 2015.

[80] C. Guo and C. Zhao, "A new technology for HVDC start-up and operation using VSC-HVDC system," in *IEEE Power Energy Soc. Gen. Meeting*, Jul. 2009, pp. 1–5.

[81] G. Li, C. Zhao, X. Zhang, and G. Li, "Research on 'soft start-up' of VSC-HVDC in power system restoration after blackouts," in *2nd IEEE Conf. Ind. Electron. and Appl.*, May 2007, pp. 1939–1943.

[82] Y. Jiang-Hafner, H. Duchen, M. Karlsson, L. Ronstrom, B. Abrahamsson, "HVDC with voltage source converters—A powerful standby black start facility," in *IEEE PES Trans. Distrib. Conf.*, Apr. 2008, pp. 1–9.

[83] K. Li and C. Zhao, "New technologies of modular multilevel converter for VSC-HVDC application," in *Power Energy Eng. Conf. (APPEEC)*, Mar. 2010, pp. 1–4.

[84] T. Li, C. Zhao, J. Xu, X. Cai, and C. Lin, "Start-up scheme for HVDC system based on modular multilevel converter," in *2nd IET Renew. Power Gen. Conf.*, Sept. 2013, pp. 1–4.

[85] K. Shi, F. Shen, D. Lv, P. Lin, M. Chen, and D. Xu, “A Novel Startup Scheme for Modular Multilevel Converter,” in *Proc. IEEE Energy Convers. Congr. Expo.*, 2012, pp. 4180–4187.

[86] M. Kong, Y. Qiu, Z. He, W. He, and J. Liu, “Pre-charging control strategies of modular multilevel converter for VSC-HVDC,” *Power Syst. Tech.*, vol. 35, no. 11, Nov. 2011 (in Chinese).

[87] X. Li, Z. Yuan, J. Fu, Y. Wang, T. Liu, and Z. Zhu, “Nanao multi-terminal VSC-HVDC project for integrating large-scale wind generation,” in *IEEE Power Energy Soc. Gen. Meeting Conf. Expo.*, Jul. 2014, pp. 1–5.

[88] P. Kundur, N. J. Balu, and M. G. Lauby, *Power System Stability and Control*, McGrawhill, 1994.

[89] X.-P. Zhang, C. Rehtanz, and B. Pal, *Flexible AC Transmission Systems: Modelling and Control*, Springer, 2006.

[90] X. Chen, C. Zhao, and C. Cao, “Research on the fault characteristics of HVDC based on modular multilevel converter,” in *IEEE Electri. Power Energy Conf. (EPEC)*, Oct. 2011, pp. 91–96.

[91] J. A. Suul, A. Luna, and P. Rodríguez, “Power control of VSC HVDC converters for limiting the influence of AC unbalanced faults on multi-terminal DC grids,” in *Proc. IET 10th Int. Conf. AC/DC Power Transmission*, Dec. 2012, pp. 1–7.

[92] Q. Tu, Z. Xu, Y. Chang, and L. Guan, “Suppressing DC voltage ripples of MMC-HVDC under unbalanced grid conditions,” *IEEE Trans. Power Del.*, vol. 27, no. 3, pp. 1332–1338, Jul. 2012.

[93] X. Shi, Z. Wang, B. Liu, Y. Liu, L. M. Tolbert, and F.Wang, “Characteristic investigation and control of modular multilevel converter based HVDC system under single-line-to-ground fault conditions,” *IEEE Trans. Power Electron.*, vol. pp, no. 99, pp. 1–12, May. 2014.

[94] G. P. Adam, K. H. Ahmed, S. J. Finney, and B. W. Williams, “AC fault ride-through capability of a VSC-HVDC transmission systems,” in *IEEE Energy Conv. Cong. Expo. (ECCE)*, Sept. 2010, pp. 3739–3745.

[95] G. P. Adam, K. H. Ahmed, S. J. Finney, K. Bell, and B. W. Williams, "New breed of network fault-tolerant voltage-source-converter HVDC transmission system," *IEEE Trans. Power Syst.*, vol. 28, no. 1, pp. 335–346, Feb. 2013.

[96] J. I. Marvik and H. G. Svendsen, "Analysis of grid faults in offshore wind farm with HVDC connection," *Energy Procedia*, vol. 35, pp. 81–90, 2013.

[97] C. Feltes, H. Wrede, F. W. Koch, and I. Erlich, "Enhanced fault ride through method for wind farms connected to the grid through VSC-based HVDC transmission," *IEEE Trans. Power Syst.*, vol. 24, no. 3, pp. 1537–1546, Aug. 2009.

[98] P. H. Huang, M. S. El Moursi, W. Xiao, and J. Kirtley, "Novel fault ride through configuration and transient management scheme for doubly fed induction generator," *IEEE Trans. Energy Convers.*, vol. 28, no. 1, pp. 86–94, Mar. 2013.

[99] B. Silva, C. L. Moreira, H. Leite, and J. A. P. Lopes, "Control strategies for AC fault ride through in multiterminal HVDC grids," *IEEE Trans. Power Del.*, vol. 29, no. 1, pp. 395–405, Jan. 2014.

[100] M. Hadjikypris and V. Terzija, "Transient fault studies in a multi-terminal VSC-HVDC grid utilizing protection means through DC circuit breakers," in *IEEE PowerTech*, Jun. 2013, pp. 1–6.

[101] M. Hadjikypris and V. Terzija, "Dynamic fault studies of an offshore four-terminal VSC-HVDC grid utilizing protection means through AC/DC circuit breakers," presented in *Power Options Eastern Mediterranean Region (POEM)*, Oct. 2013.

[102] J. Yang, J. Zheng, G. Tang, and Z. He, "Characteristics and recovery performance of VSC-HVDC DC transmission line fault," in *Power Energy Eng. Conf. (APPEEC)*, Mar. 2010, pp. 1–4.

[103] J. Rafferty, L. Xu, and J. Morrow, "Analysis of voltage source converter-based high-voltage direct current under DC line-to-earth fault," *IET Power Electron.*, vol. 8, no. 3, pp. 428–438, Mar. 2015.

[104] J. Yang, J. E. Fletcher, and J. O'Reilly, "Multiterminal dc wind farm collection grid internal fault analysis and protection scheme design," *IEEE Trans. Power Del.*, vol. 25, no. 4, pp. 2308–2318, Oct. 2010.

[105] J. Descloux, P. Rault, S. Nguefeu, J.-B. Curis, X. Guillaud, F. Colas, B. Raison, "HVDC meshed grid: control and protection of a multi-terminal HVDC system," *Cigré Paper*, B4–308, 2012.

[106] W. Leterme, P. Tielens, S. De Boeck, and D. Van Hertem, "Overview of grounding and configuration options for meshed HVDC grids," *IEEE Trans. Power Del.*, vol. 29, no. 6, pp. 2467–2475, Dec 2014.

[107] L. Tang and B.-T. Ooi, "Protection of VSC-multi-terminal HVDC against DC faults," in *IEEE 33rd Annual Power Electron. Spec. Conf.*, vol.2, 2002, pp. 719–724.

[108] L. Tang and B.-T. Ooi, "Locating and isolating dc faults in multi-terminal dc systems," *IEEE Trans. Power Del.*, vol. 22, no. 3, pp. 1877–1884, Jul. 2007.

[109] K. D. Kerf, K. Srivastava, M. Reza, D. Bekaert, S. Cole, D. V. Hertem, and R. Belmans, "Wavelet-based protection strategy for DC faults in multi-terminal VSC HVDC systems," *IET Gen. Transm. Distrib.*, vol. 5, no. 4, pp. 496–503, Apr. 2011.

[110] D. Yu, Y. Li, Y. Ding, and X. Zhang, "Fault detection and location for MTDC combining wavelet analysis and travelling wave," in *IEEE Power Eng. Auto. Conf. (PEAM)*, Sept. 2012, pp. 1–4.

[111] M. Callavik, A. Blomberg, J. Häfner, and B. Jacobson, "The hybrid HVDC breaker," ABB Grid Systems Technical Paper, Nov. 2012.

[112] K. Sano and M. Takasaki, "A surgeless solid-state DC circuit breaker for voltage-source-converter-based HVDC systems," *IEEE Trans. Ind. Appl.*, vol. 50, no. 4, pp. 2690–2699, Jul. 2014.

[113] C. C. Davidson, R. S. Whitehouse, C. D. Barker, J.-P. Dupraz, and W. Grieshaber, "A new ultra-fast HVDC circuit breaker for meshed DC networks," in *Proc. IET 11th Int. Conf. AC/DC Power Transmission*, Feb. 2015.

[114] C. Y. Zhao, J. Xu, and T. Li, "DC faults ride-through capability analysis of full-bridge MMC-MTDC system," *Sci. China Tech. Sci.*, vol. 56, pp. 253–261, Jan. 2013.

[115] R. Feldman, E. Farr, A. J. Watson, J. C. Clare, P. W. Wheeler, D. R. Trainer, and R. W. Crookes, "DC fault ride-through capability and STATCOM operation of a HVDC

hybrid voltage source converter," *IET Gen. Transm. Distrib.*, vol. 8, no. 1, pp. 114–120, Jan. 2014.

[116] J. Wu, S. Zhang, and D. Xu, "Modeling and control of multi-terminal HVDC with offshore wind farm integration and DC chopper based protection strategies," in *IEEE 39th Annual Conf. Ind. Electron. Soc. (IECON)*, Nov. 2013, pp. 1013–1018.

[117] N. Yousefpoor, A. Narwal, and S. Bhattacharya, "Control of DC-fault-resilient voltage source converter based HVDC transmission system under DC fault operating condition," *IEEE Trans. Ind. Electron.*, vol. PP, no. 99, Nov. 2014.

[118] A. A. Elserougi, A. M. Massoud, A. S. Abdel-Khalik, and S. Ahmed, "Bidirectional buck-boost inverter-based HVDC transmission system with AC-side contribution blocking capability during DC-side faults," *IEEE Trans. Power Del.*, vol. 29, no. 3, pp. 1249–1261, Jun. 2014.

[119] X. Li, Q. Song, W. Liu, H. Rao, S. Xu, and L. Li, "Protection of nonpermanent faults on DC overhead lines in MMC-Based HVDC systems," *IEEE Trans. Power Del.*, vol. 28, no. 1, pp. 483–490, Jan. 2013.

[120] H. Zeng, Y. Zhu, and J. Liu, "Verification of DFIG and PMSG wind turbines' LVRT characteristics through field testing," in *IEEE Int. Conf. Power Syst. Tech. (POWERCON)*, New Zealand, Nov. 2012.

[121] M. Mohseni, S. M. Islam and M. A. S. Masoum, "Impacts of symmetrical and asymmetrical voltage sags on DFIG-based wind turbines considering phase-angle jump, voltage recovery, and sag parameters," *IEEE Trans. Power Electron.*, vo1. 26, no. 5, pp. 1587–1597, May 2011.

[122] G. Pannell, D. J. Atkinson and B. Zahawi, "Analytical study of grid-fault response of wind turbine doubly fed induction generator," *IEEE Trans. Power Convers.*, vo1. 25, no. 4, pp. 1081–1091, Dec. 2010.

[123] Z. Chen, J. M. Guerrero and F. Blaabjerg, "A review of the state of the art of power electronics for wind turbines," *IEEE Trans. Power Electron.*, vo1. 24, no. 8, pp. 1859–1875, Aug. 2009.

[124] M. A.-Salam, A. Ahmed, and M. Mahrous, "Transient analysis of grid connected wind driven PMSG, DFIG and SCIG at fixed and variable speeds", *Innovative Syst. Design Eng.*, vol. 2, no. 3, pp. 1–19, 2011.

[125] R. Pena, J. C. Clare, and G. M. Asher, "Doubly fed induction generator using back-to-back PWM converters and its application to variable-speed wind-energy generation," *Proc. Inst. Elect. Eng.*, vol. 143, no. 3, pp. 231–241, May 1996.

[126] *RTDS user's documentation: Wind-turbine driven doubly-fed induction generator*, RTDS Technologies, 2011.

[127] Low Voltage Ride Through, Wikipedia, available online at: https://en.wikipedia.org/-wiki/Low_voltage_ride_through

[128] J. Morren and S. W. H. de Haan, "Ridethrough of wind turbines with doubly-fed induction generator during a voltage dip," *IEEE Trans. Energy Convers.*, vol. 20, no. 2, pp. 435–441, Jun. 2005.

[129] M. Mohseni, M. A. S. Masoum, and S. M. Islam, "Low and high voltage ride-through of DFIG wind turbines using hybrid current controlled converters," *Electr. Power Syst. Res.*, vol. 81, no. 7, pp. 1456–1465, Jul. 2011.

[130] *The Grid Code, Issue 5, Revision 13*, National Grid Electricity Transmission plc, Great Britain, Jan 2015, available online at http://www.nationalgrid.com/uk.

[131] A. Timofejevs and D. Gamboa, "Control of MMC in HVDC applications," Master dissertation, Aalborg University, Aalborg, Denmark, 2013.

[132] T. K. Vrana, Y. Yang, D. Jovcic, S. Dennetiere, J. Jardini, and H. Saad, "The CIGRE B4 DC grid test system," *CIGRE Electra Magazine*, vol.270, Oct. 2013, pp. 10–19.

[133] P. Wang, X. P. Zhang, P. F. Coventry, and R. Zhang, "Start-up control of an offshore integrated MMC multi-terminal HVDC system with reduced DC voltage," *IEEE Trans. Power Syst.*, DOI: 10.1109/TPWRS.2015.2466600 (accepted for publication).

[134] A. Yazdani and R. Iravani, "Dynamic model and control of the NPC-based back-to-back HVDC system," *IEEE Trans. Power Del.*, vol. 21, no. 1, pp. 414–424, Jan. 2006.

[135] P. Wang, Z. Li, X. P. Zhang, R. Zhang and P. F. Coventry, "DC fault management for VSC MTDC system using delayed-auto-re-configuration scheme," in *Proc. 11th IET Int. Conf. on AC and DC Power Transmission*, Feb. 2015.

[136] P. Wang, X. P. Zhang, R. Zhang, P. F. Coventry, and Z. Li, "Control and protection sequence for recovery and reconfiguration of an offshore integrated MMC multi-terminal HVDC system under DC faults," *Int. J. Electrical Power & Energy Syst.*, (submitted and currently under review).

[137] P. Wang, X. P. Zhang, N. Deng, P. F. Coventry and R. Zhang, "Control and protection sequence of an offshore integrated MMC MTDC system with master-slave/droop control under converter AC-side fault," in *6th Int. Conf. on Advanced Power Syst. Auto. Protection (APAP 2015)*, Sept. 2015, pp. 1–5.

[138] P. Wang, X. P. Zhang, P. F. Coventry and Z. Li, "Control and protection strategy for MMC MTDC system under converter-side AC fault during converter blocking failure," *J. Modern Power Syst. Clean Energy*, vol. 2, no. 3, pp. 272–281, Sept. 2014.

[139] Z. Y. He, L. Fu, S. Lin, and Z. Q. Bo, "Fault detection and classification in EHV transmission line based on wavelet singular entropy," *IEEE Trans. Power Del.*, vol. 25, no. 4, pp. 2156–2163, Oct. 2010.

[140] J. A. Jiang, C. L. Chuang, Y. C. Wang, C. H. Hung, J. Y. Wang, C. H. Lee, and Y. T. Hsiao, "A hybrid framework for fault detection, classification, and location Part I: Concept, structure, and methodology," *IEEE Trans. Power Del.*, vol. 26, no. 3, pp. 1988–1997, Jul. 2011.

[141] P. Mahat, Z. Chen, B. Bak-Jensen, and C. Bak, "A simple adaptive overcurrent protection of distribution systems with distributed generation," *IEEE Trans. Smart Grid*, vol. 2, no. 3, pp. 428–437, Sep. 2011

[142] P. Nuutinen, P. Peltoniemi, and P. Silventoinen, "Short-circuit protection in a converter-fed low-voltage distribution network," *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 1587–1597, Apr. 2013.

[143] S. Dambhare, S. Soman, and M. Chandorkar, "Adaptive current differential protection schemes for transmission-line protection," *IEEE Trans. Power Del.*, vol. 24, no. 4, pp. 1832–1841, Oct. 2009.

[144] P. Cairoli, R. A. Dougal, and K. Lentijo, "Coordination between supply power converters and contactors for fault protection in multi-terminal MVDC distribution systems," in *IEEE Electric Ship Tech. Sympo. (ESTS)*, pp. 493–499, Apr. 2013.

[145] P. K. Dutta and P. B. DuttaGupta, "Novel signal processing techniques for fault detection and location in HV subtransmission and transmission lines," in *2nd Int. Conf. Advances Power Syst. Control, Operation and Management (APSCOM)*, pp. 673–678, Dec. 1993.

[146] Y.-Y. Hong, Y.-H. Wei, Y.-R. Chang, Y.-D. Lee, and P.-W. Liu, "Fault detection and location by static switches in microgrids using wavelet transform and adaptive network-based fuzzy inference system," *Energies*, vol. 7, no. 4, pp. 2658–2675, Apr. 2014.

[147] "Simulation of multi-terminal VSC HVDC system by means of real time digital simulator (RTDS)," Project Report for National Grid, Dec. 2013.

[148] B. Dellby, G. Bergman, J. Karlstrand, and J. Kaumanns, "High-voltage cable technology," *ABB Rev.*, vol. 4, pp. 35–44, 2000.

[149] *RTDS official website: HVDC & FACTS applications*, RTDS Technologies, available online at: https://www.rtds.com/applications/hvdc-and-facts/

[150] *RTDS user's documentation: VSC modular multilevel converters*, RTDS Technologies, 2014.

[151] A. Antonopoulos, L. Angquist, and H. P. Nee, "On dynamics and voltage control of the modular multilevel converter," in *13th Eur. Conf. Power Electron. Appli.*, Spain, Sept. 2009, pp. 1–10.

[152] *MATLAB SimPowerSystems documentation: Wind turbine*, Mathworks, 2004.

[153] J. G. Slootweg, S. W. H. De Hann, H. Polinder, and W. L. Kling, "General model for representing variable speed wind turbines in power system dynamic simulations," *IEEE Trans. Power Syst.*, vol. 18, no. 1, pp. 144–151, Feb. 2003.

[154] D. Woodford, "Determination of Main Parameters for a Doubly Fed Induction Generator for a Given Turbine Rating," *Electranix Technical Paper*, 2004.